

MI40-030

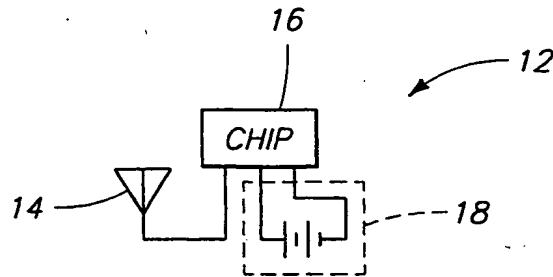


FIG. 1

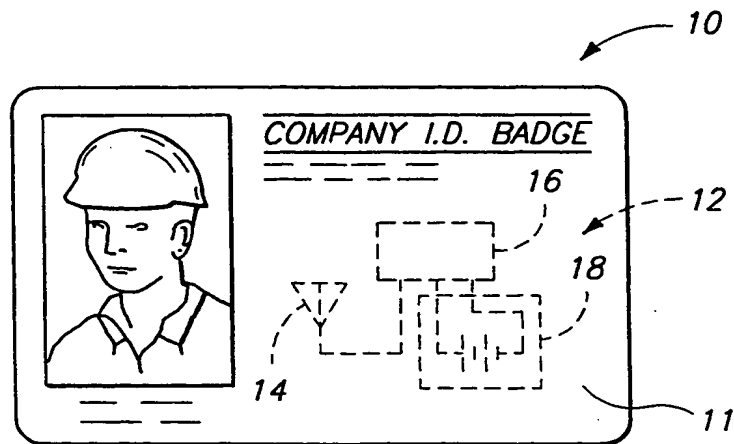


FIG. 2

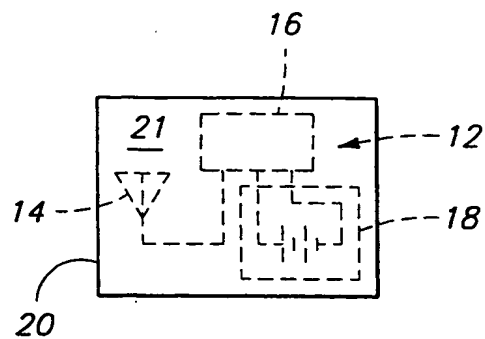


FIG. 1

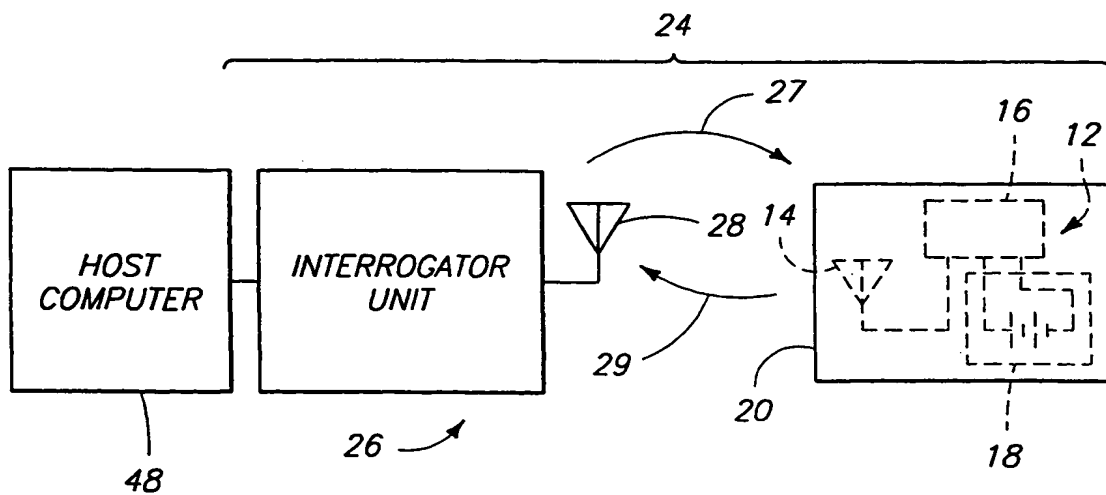
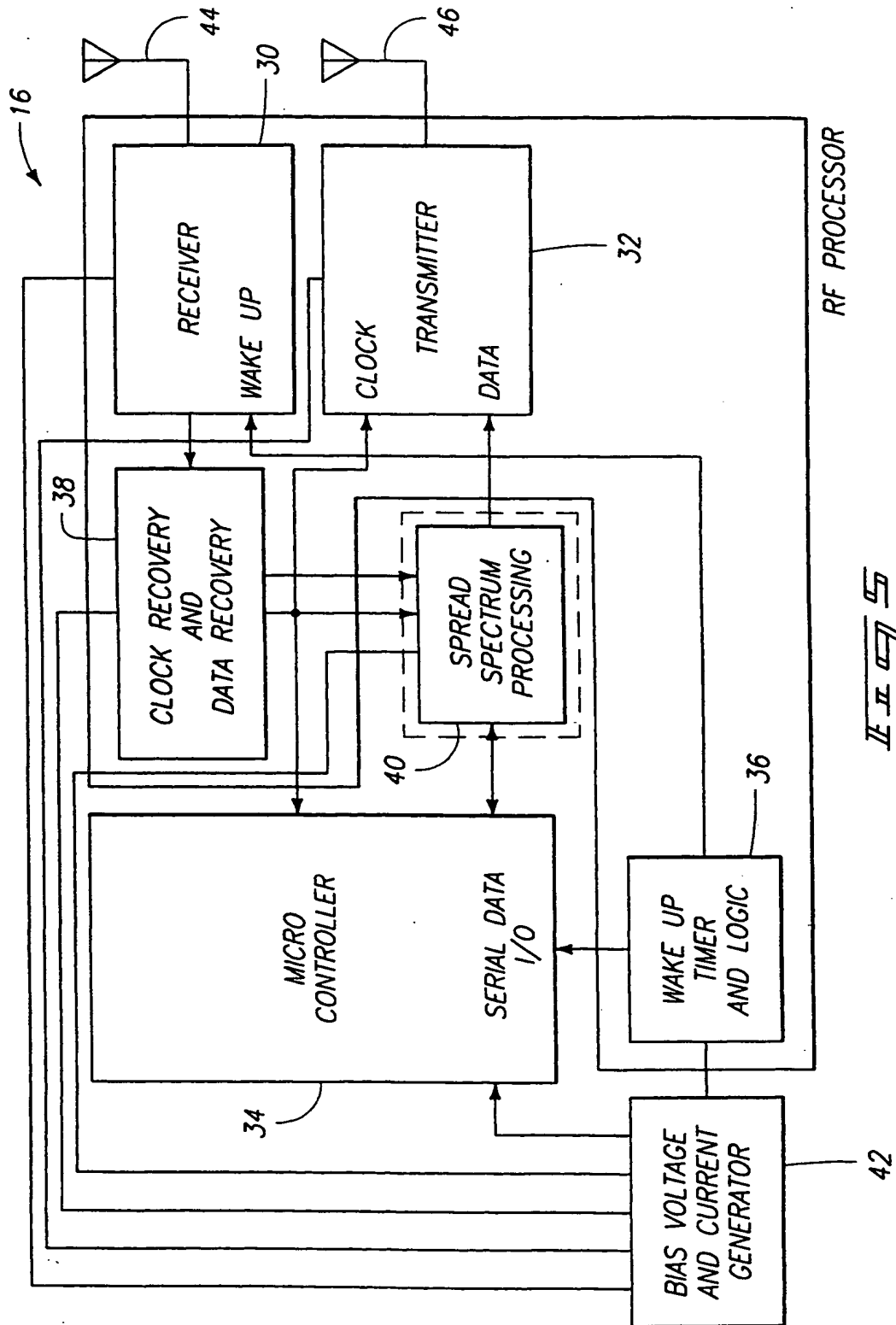


FIG. 2

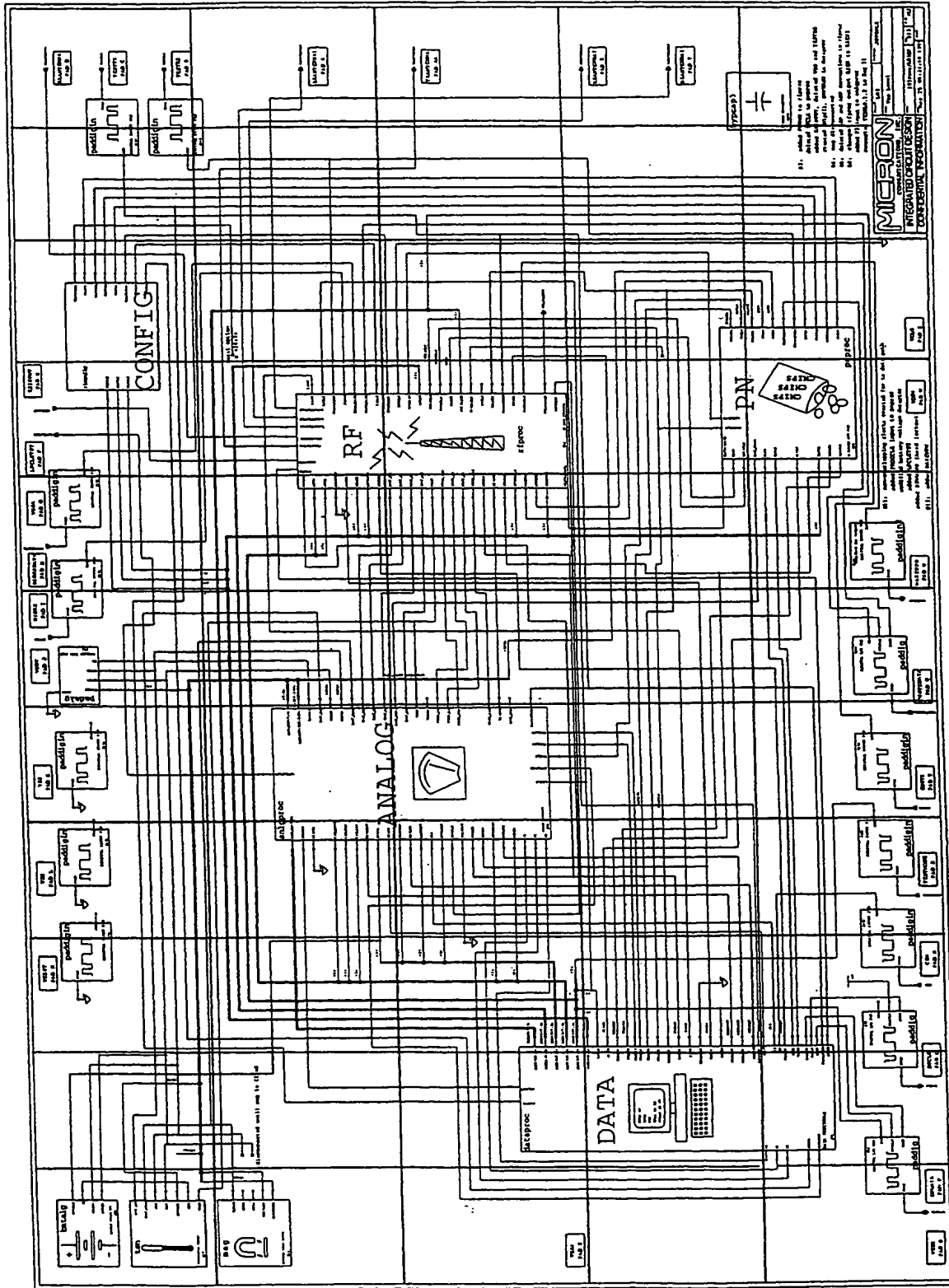


6AA	6AB	6AC	6AD	6AE	6AF	6AG	6AH	6AI	6AJ	6AK
6BA	6BB	6BC	6BD	6BE	6BF	6BG	6BH	6BI	6BJ	6BK
6CA	6CB	6CC	6CD	6CE	6CF	6CG	6CH	6CI	6CJ	6CK
6DA	6DB	6DC	6DD	6DE	6DF	6DG	6DH	6DI	6DJ	6DK
6EA	6EB	6EC	6ED	6EE	6EF	6EG	6EH	6EI	6EJ	6EK

MI 40-030



FIG. 6AA-EK



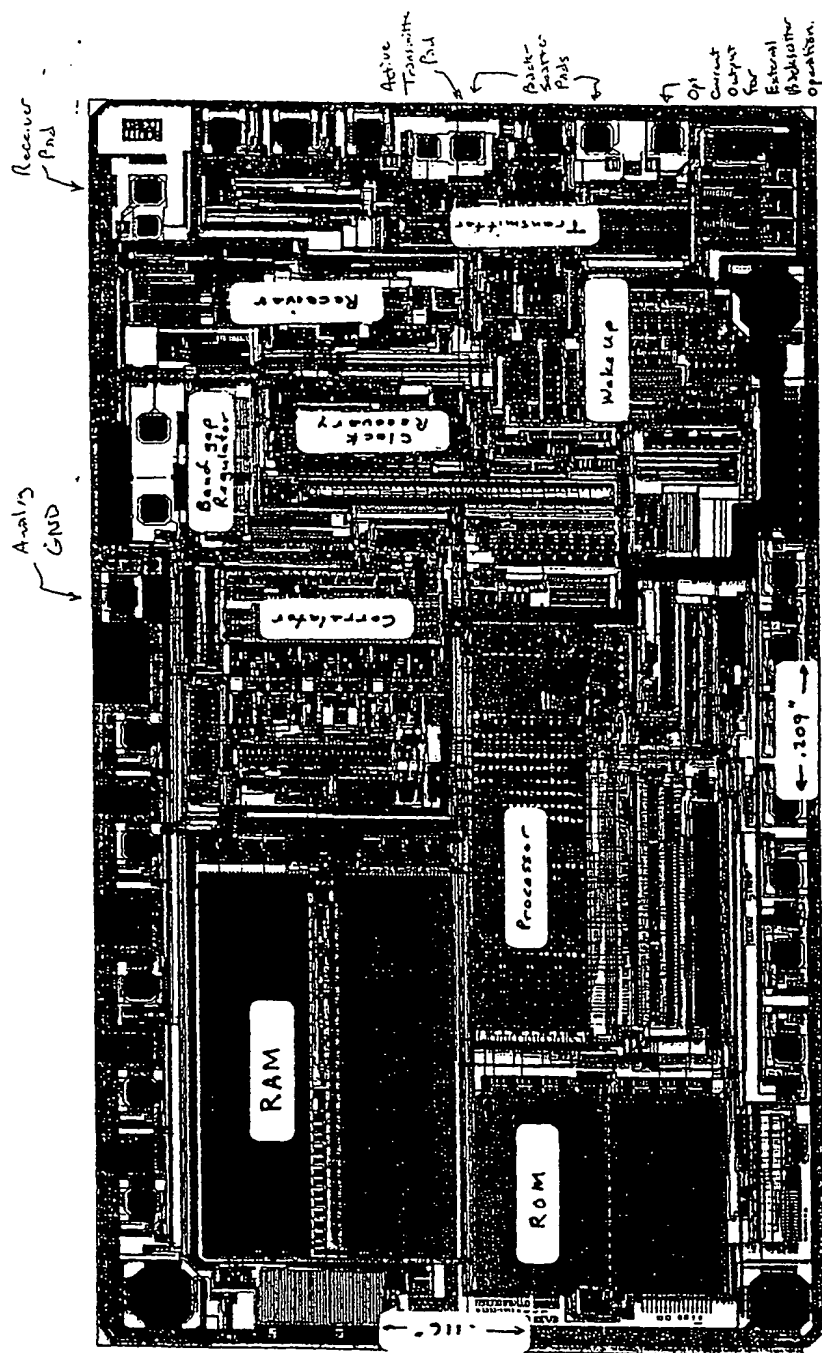
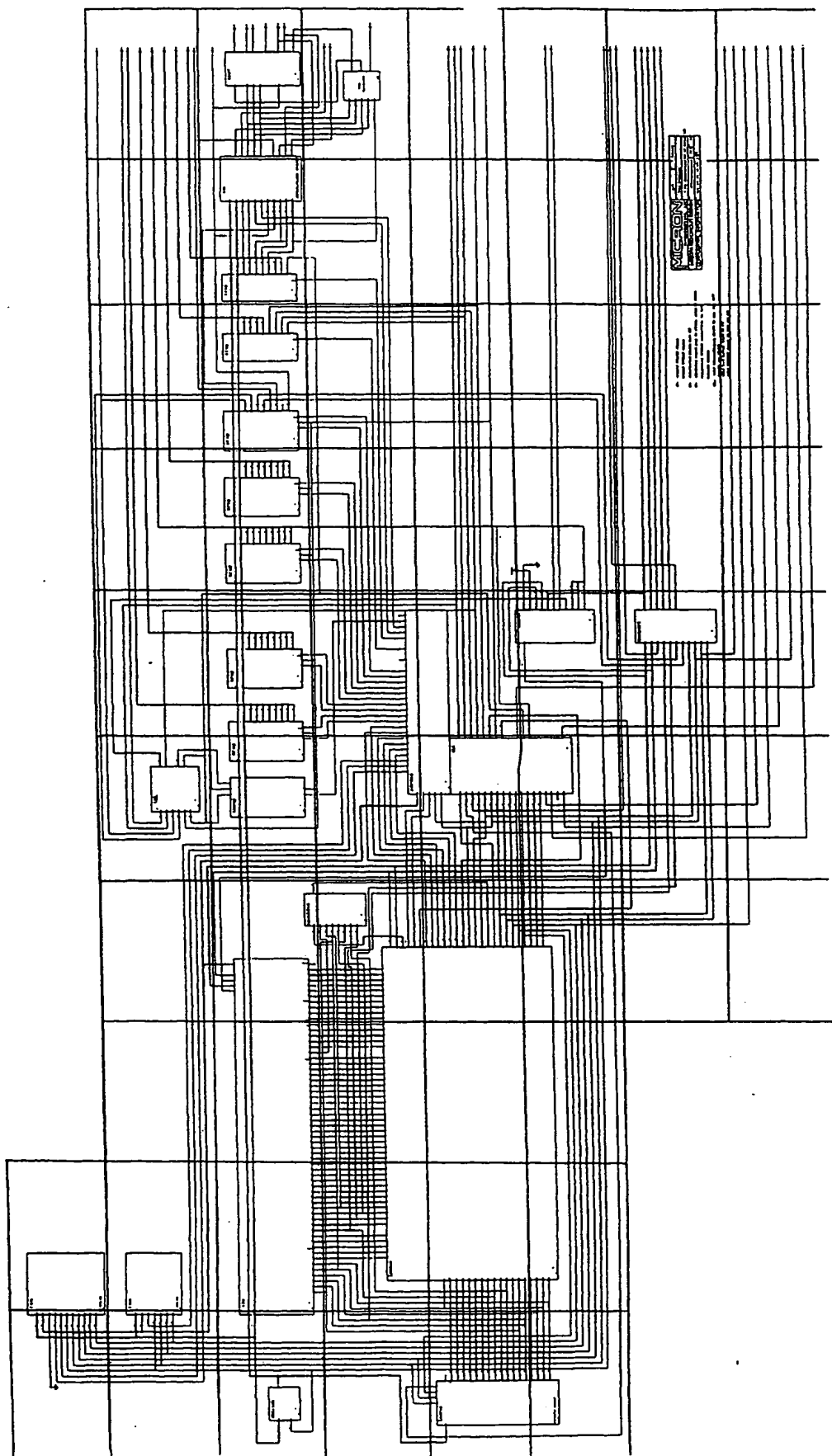


FIG. 6.01

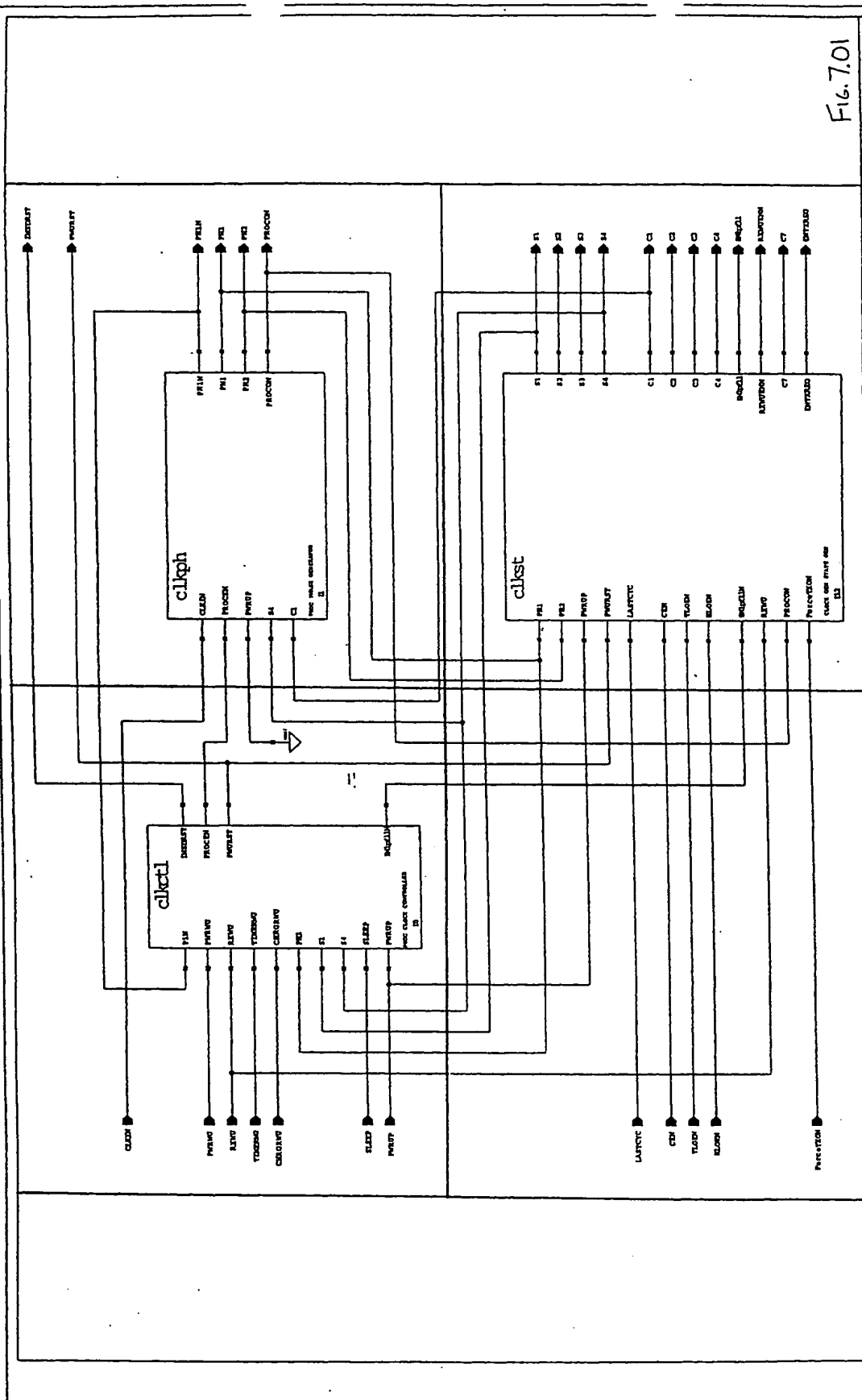
7AA	7AB		7BD	7BE	7BF	7BG	7BH	7BI	7BJ
7BA	7BB	7BC	7BD	7BE	7BF	7BG	7BH	7BI	7BJ
7CA	7CB	7CC	7CD	7CE	7CF	7CG	7CH	7CI	7CJ
7DA	7DB	7DC	7DD	7DE	7DF	7DG	7DH	7DI	7DJ
7EA	7EB	7EC	7ED	7EE	7EF	7EG	7EH	7EI	7EJ
7FA	7FB	7FC	7FD	7FE	7FF	7FG	7FH	7FI	7FJ
			7GD	7GE	7GF	7GG	7GH	7GI	7GJ
			7HD	7HE	7HF	7HG	7HH	7HI	7HJ

$$\frac{\pi}{\pi + \pi}$$



7.01AA	7.01AB
7.01BA	7.01BB

EX-9 T.001



```

E2: created ENUPfall signal
    added ENTXREG logic

fall: added hard lockout to clkst

```

# NICARON

**COMMUNICATIONS, INC.**  
**INTEGRATED CIRCUIT DESIGN**

**CONFIDENTIAL INFORMATION**

Rotzoll

Generator

10/18/2010

AT&T-0/03

clk	811
-----	-----

2 1996	
--------	--

\_\_\_\_\_

7.0101AA	7.0101AB
7.0101BA	7.0101BB

U.S. DEPT. OF JUSTICE

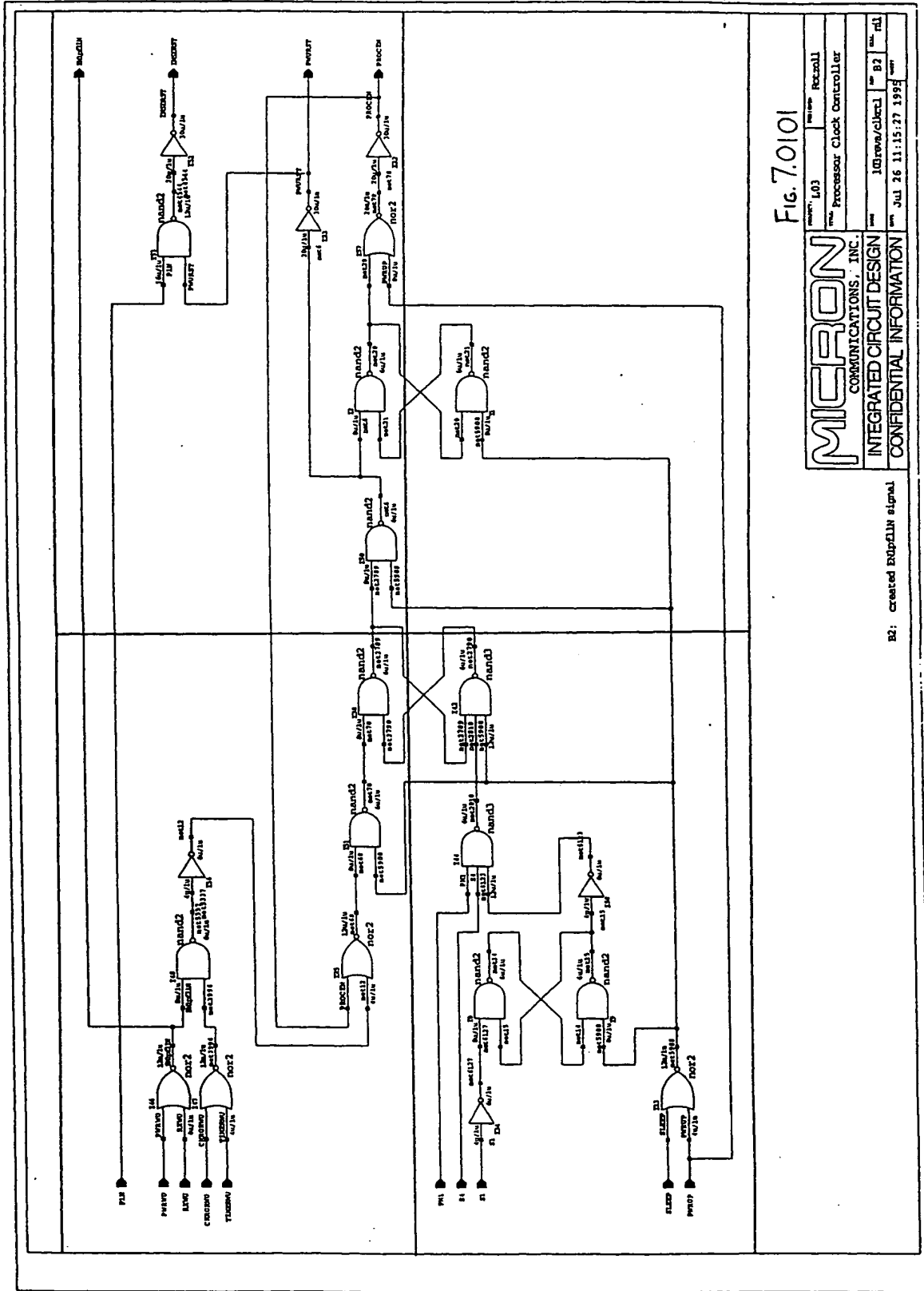


Fig. 7.0101

<b>MICRON</b> COMMUNICATIONS, INC. INTEGRATED CIRCUIT DESIGN	REV. 1.03	RECALL
	Processor Clock Controller	
	100 pins/client	92 pins
CONFIDENTIAL INFORMATION		

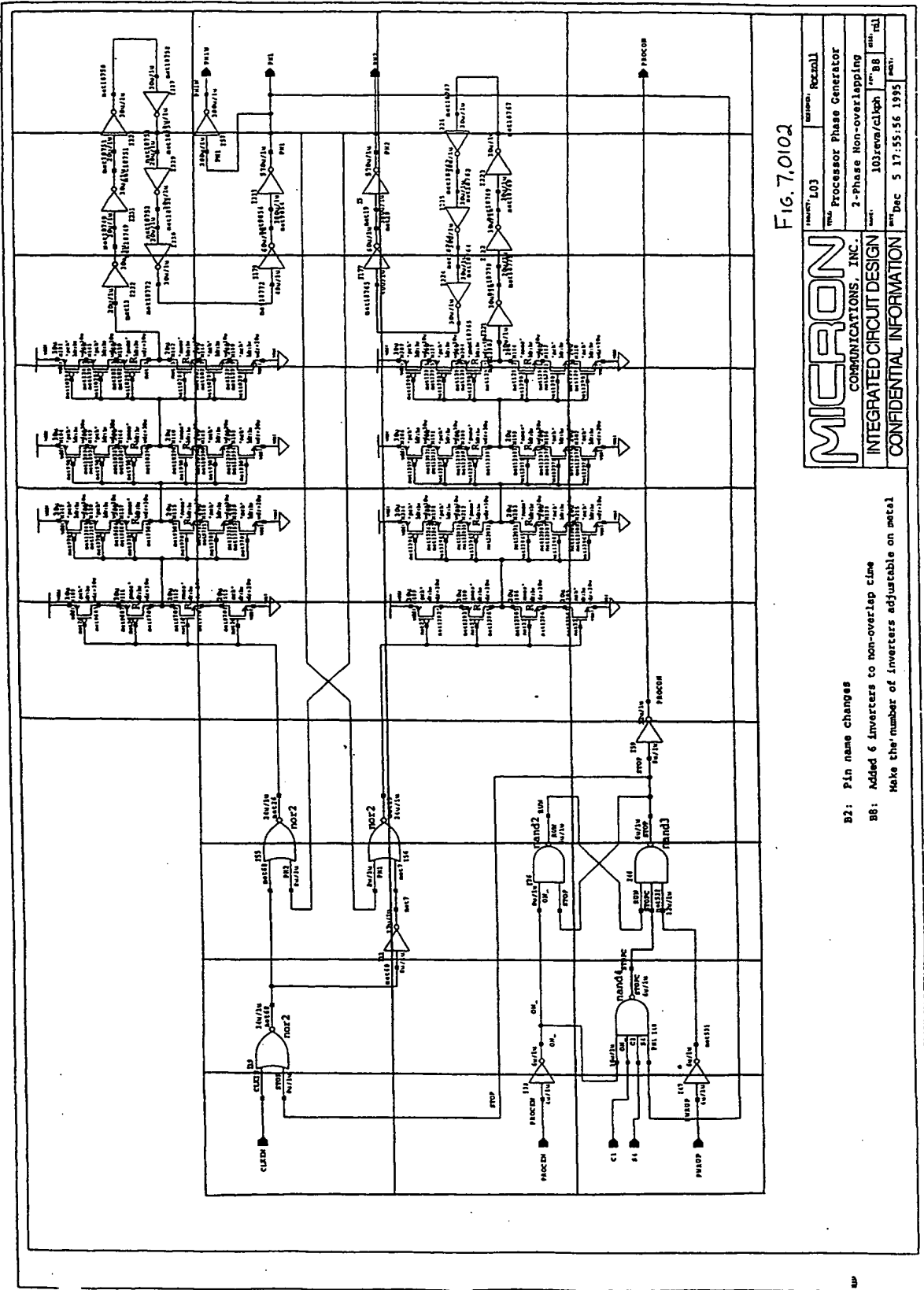
RE: created SUPPLY signal

Jul 26 11:15:27 1995



7.0102BA	7.0102BB	7.0102BC	7.0102BD	7.0102BE	7.0102BF	7.0102AG	7.0102AH	7.0102AI	7.0102AJ
7.0102CA	7.0102CB	7.0102CC	7.0102CD	7.0102CE	7.0102CF	7.0102CG	7.0102CH	7.0102CI	7.0102CJ
7.0102DA	7.0102DB	7.0102DC	7.0102DD	7.0102DE	7.0102DF	7.0102DG	7.0102DH	7.0102DI	7.0102DJ

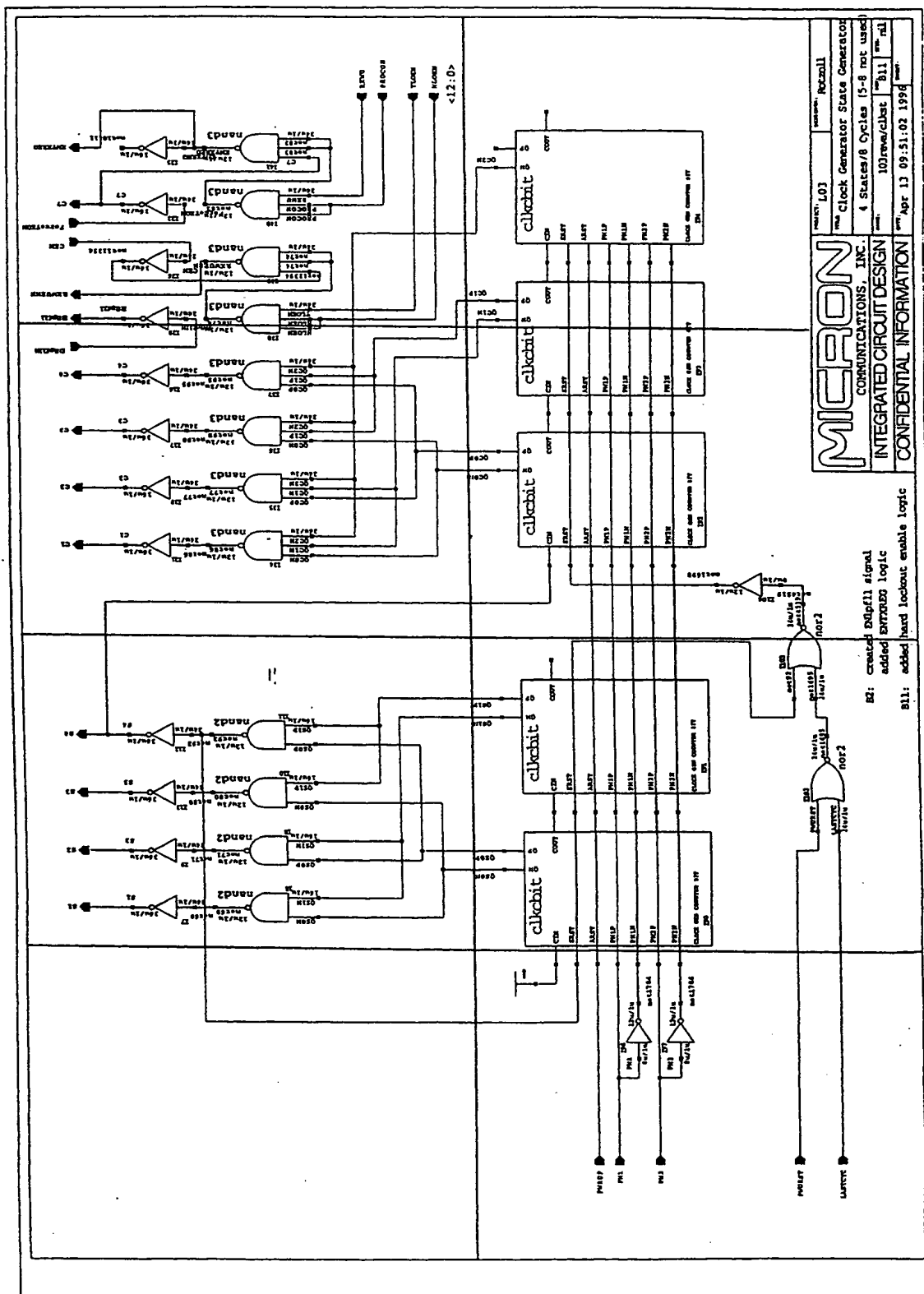
7.0102



7.0103AA	7.0103AB	7.0103AC	7.0103AD
7.0103BA	7.0103BB	7.0103BC	7.0103BD

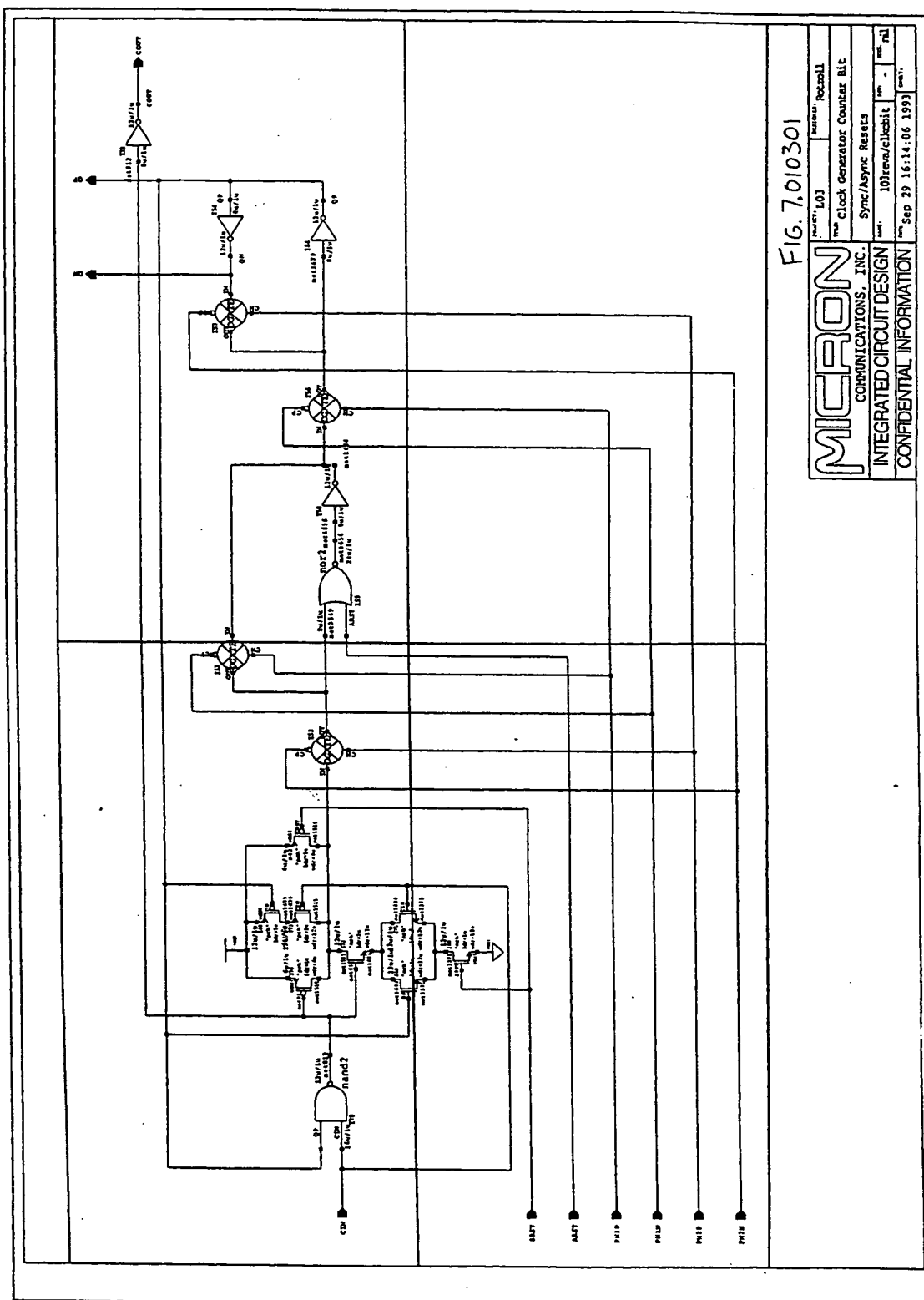
IL 100

Fig. 7.0103



7.010301AA	7.010301AB
7.010301BA	7.010301BB

SECRET



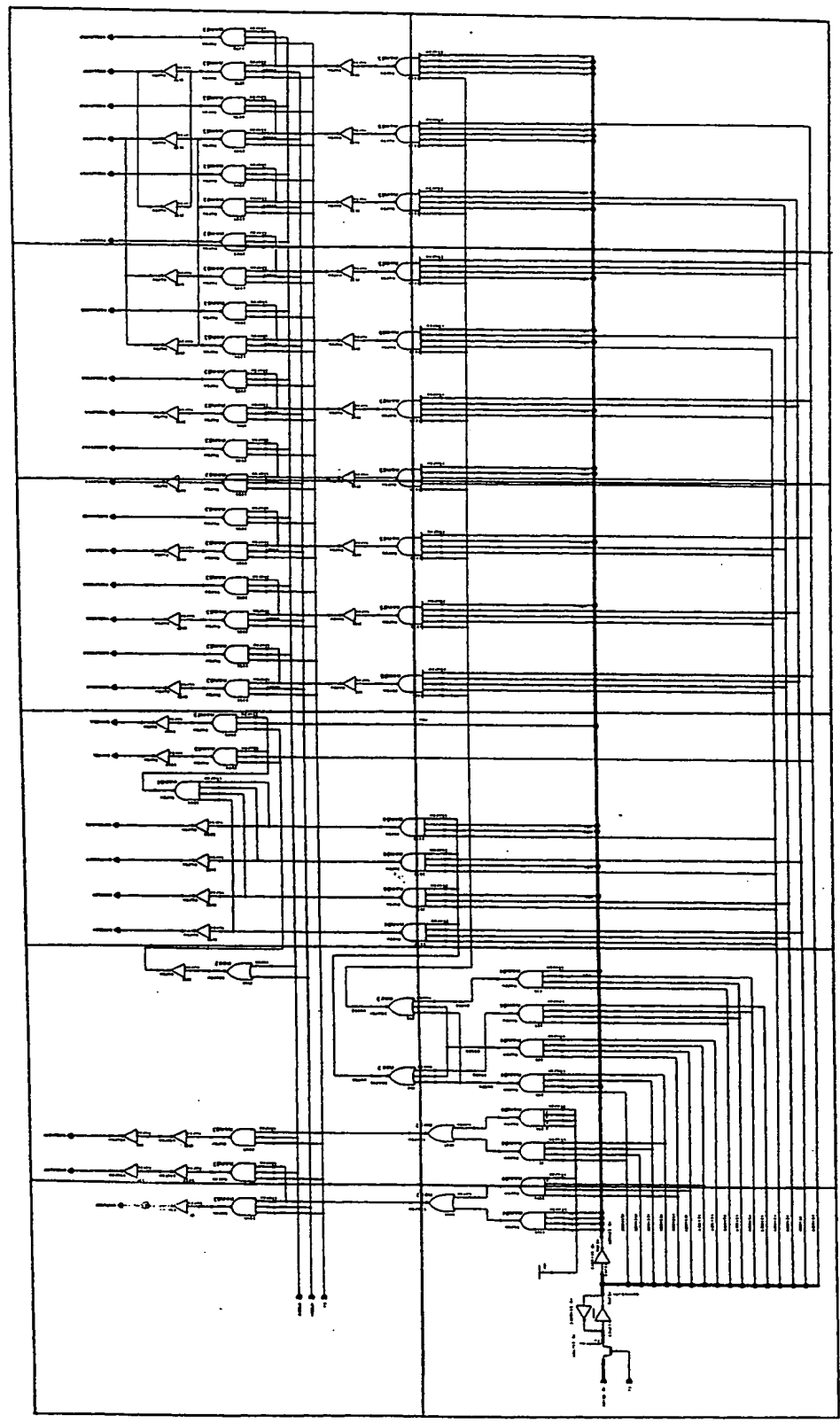
7.02AA	7.02AB	7.02AC	7.02AD	7.02AE	7.02AF
7.02BA	7.02BB	7.02BC	7.02BD	7.02BE	7.02BF

IL 11 09 11 00 00

FIG. 7.02

<b>MICRON</b>	
COMMUNICATIONS, INC.	Address: [ ]
INTEGRATED CIRCUIT DESIGN	Telephone: [ ]
CONFIDENTIAL INFORMATION	

86. 800-454-4545 at 800-454-4545

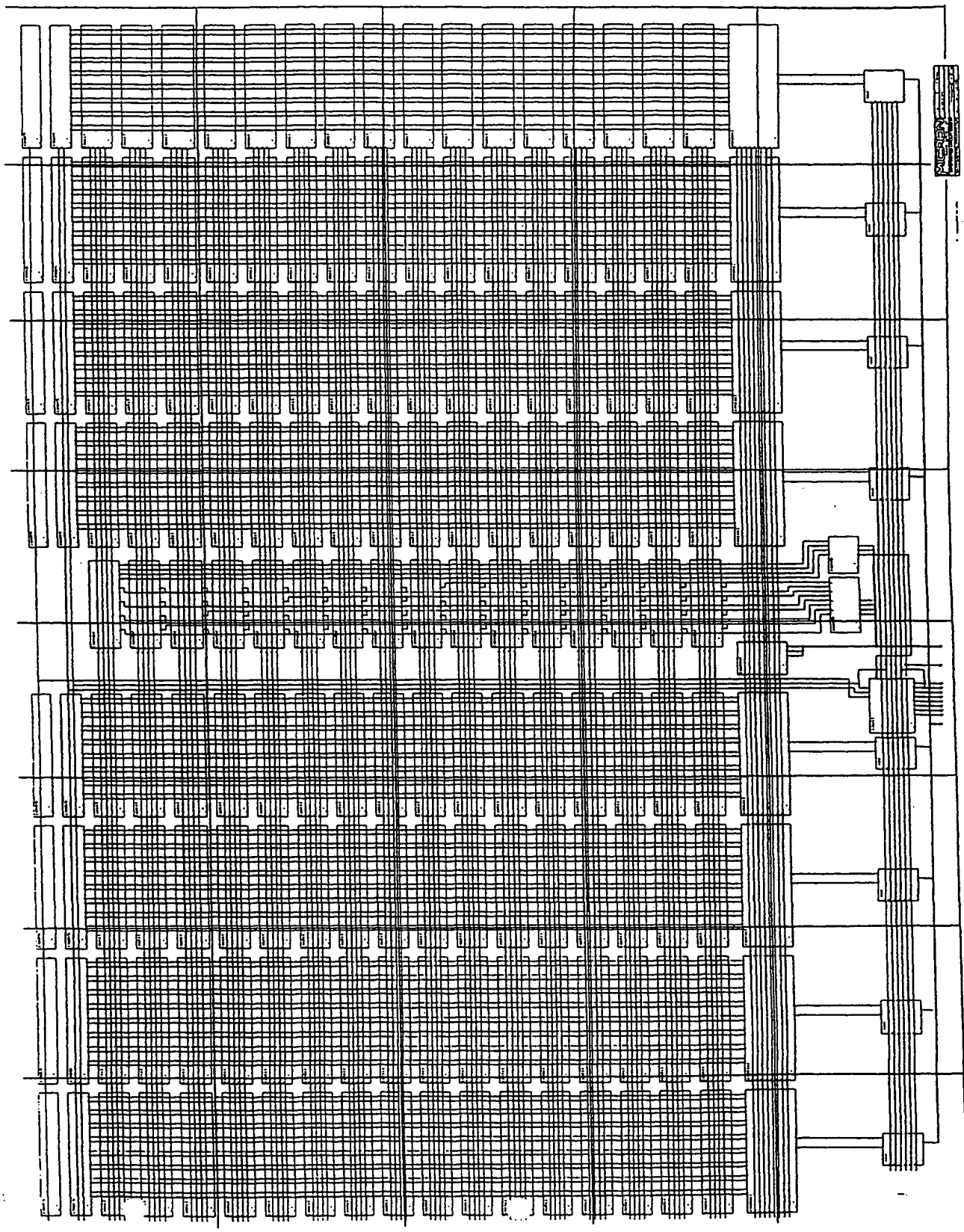




7.03AA	7.03AB	7.03AC	7.03AD	7.03AE	7.03AF	7.03AG	7.03AH
7.03BA	7.03BB	7.03BC	7.03BD	7.03BE	7.03BF	7.03BG	7.03BH
7.03CA	7.03CB	7.03CC	7.03CD	7.03CE	7.03CF	7.03CG	7.03CH
7.03DA	7.03DB	7.03DC	7.03DD	7.03DE	7.03DF	7.03DG	7.03DH
7.03EA	7.03EB	7.03EC	7.03ED	7.03EE	7.03EF	7.03EG	7.03EH

II II III IIII

Fig 7.03



7.0301AA	7.0301AB
7.0301BA	7.0301BB

THE END

Handwritten: *Handwritten*

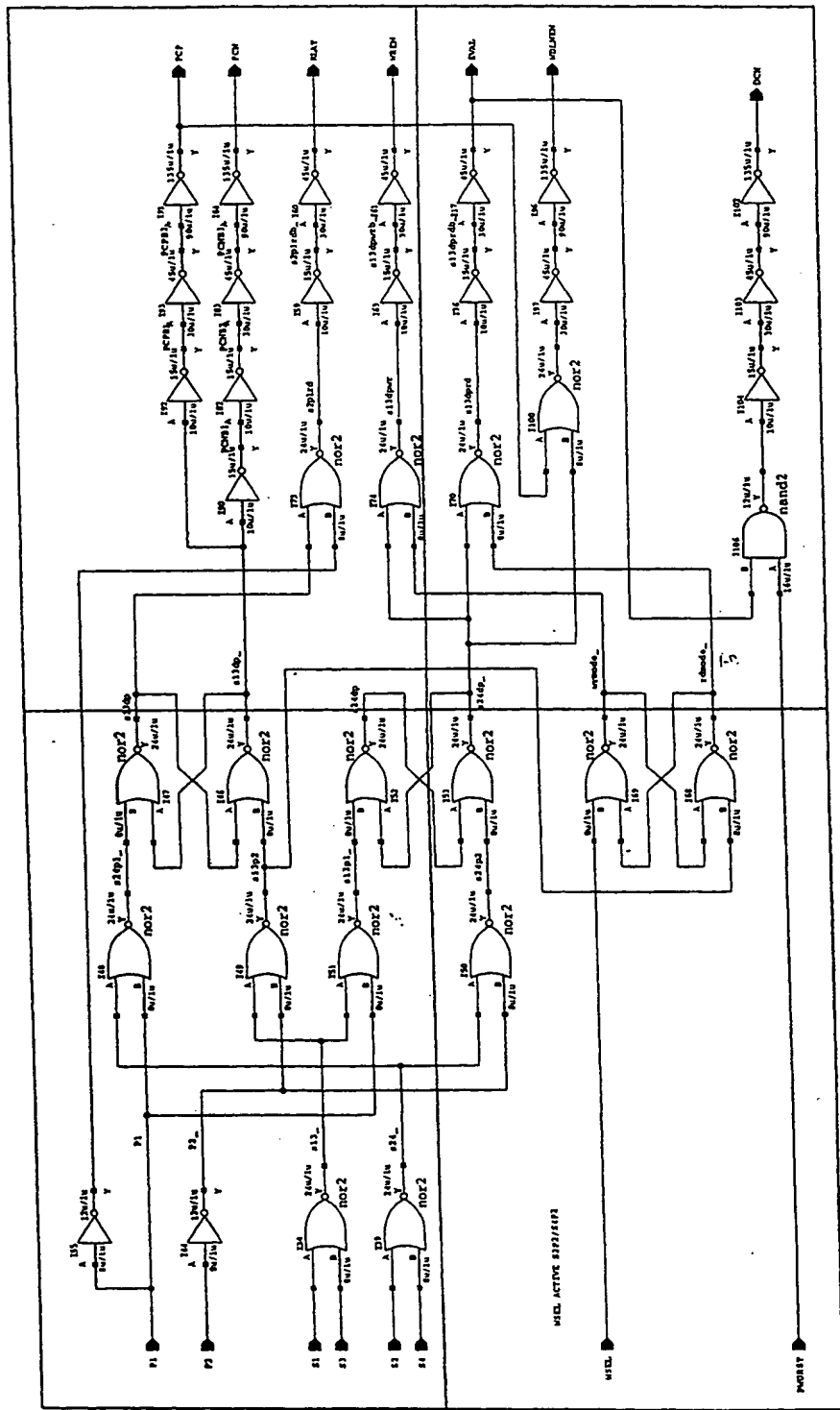


Fig. 7.0301

<b>MICRON</b>	
COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
PROJECT: 103 Af3	DESIGNED: Rozzoli
TTL RAM Control	
DATE: 10/19/74	REV: 1
DRAWN: 10/19/74	
CHECKED: 10/19/74	
DATE: Feb 11 16:47:36 1994	

7.0302AC

7.0302AB

7.0302AA

EX 7.0302

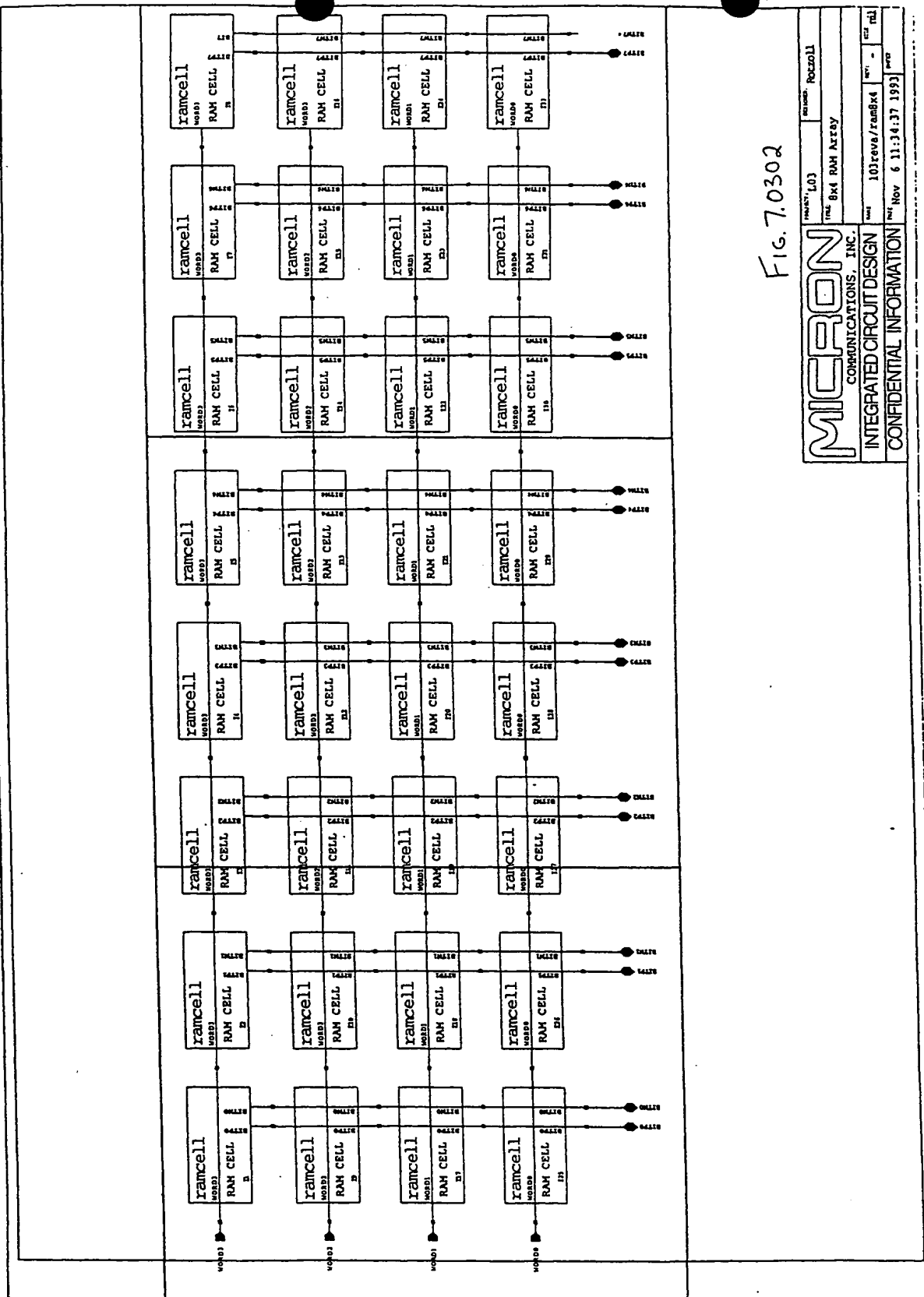


Fig. 7.0302

<b>MICRON</b>	PROJECT: L03	REVISION: Rev 001
	TYPE: 8x4 RAM Array	
	INTEGRATED CIRCUIT DESIGN	
	CONFIDENTIAL INFORMATION	

DATE: 10/18/94	DESIGNER: ram8x4	CHK: ml
TIME: 6 11:34:37 1993		REV: 001



7.0303AA	7.0303AB	7.0303AC	7.0303AD
----------	----------	----------	----------

EX-107 7.0303AD



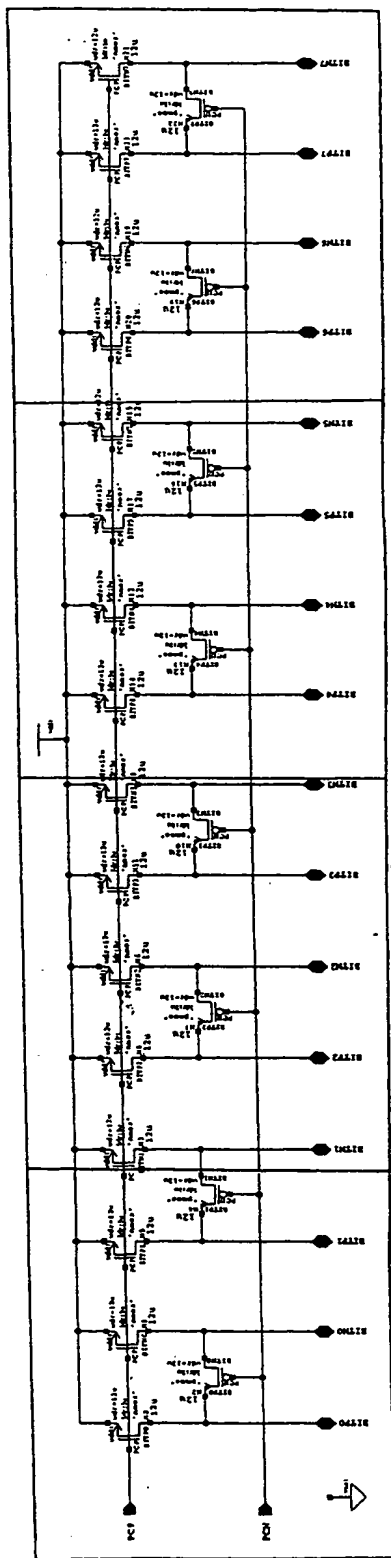


Fig. 7.0303

<b>MICRON</b> COMMUNICATIONS, INC. INTEGRATED CIRCUIT DESIGN CONFIDENTIAL INFORMATION	PART NO. L03	REVISION: Rotzoll
	TITLE: RAM Precharge	
	DESIGNED: 101revs/rampch	DATE: 11/12/93
	PRINTED: Nov 12 02:58:36 1993	

7.0304AA	7.0304AB	7.0304AC	7.0304AD
----------	----------	----------	----------

EX-70304

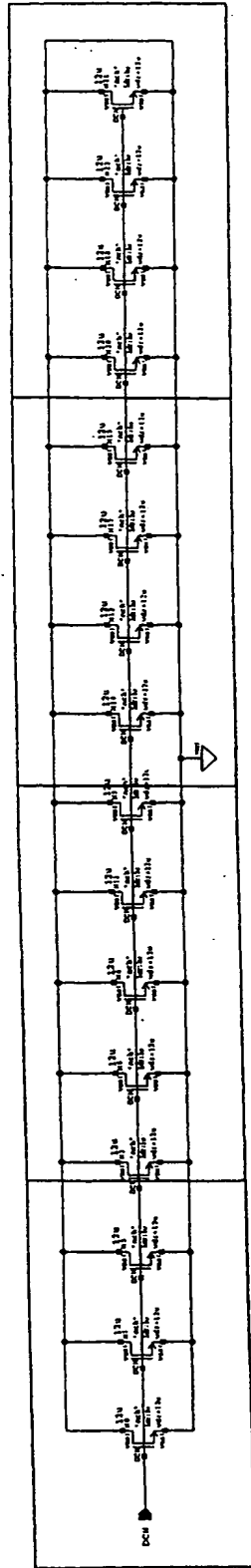


FIG. 7.0304

PROPERTY L03		MICROTON J0700LE	
NAME RAM Precharge			
DATE 10/28/94		REV. B8	
BY Jan 28 09:51:27 1996		SHEET	

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

B8: disconnected dch devices from bit lines and tied to vss

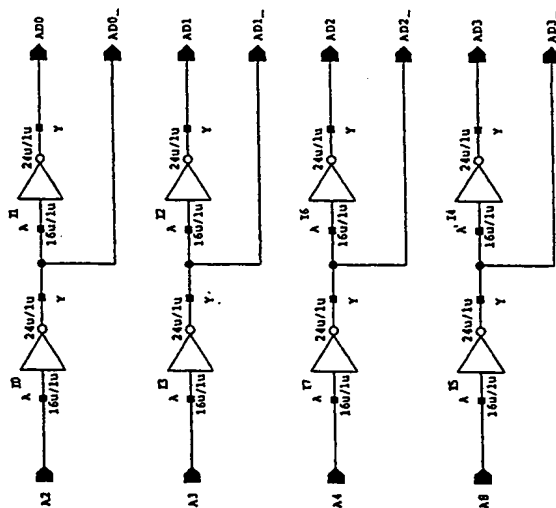


Fig. 7.0305

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: RAM Address Buffer			
NAME:	103revA/ramadb	REV:	-
DATE:	Sep 29 16:04:01 1993	SIZE:	A
CONFIDENTIAL INFORMATION			

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN

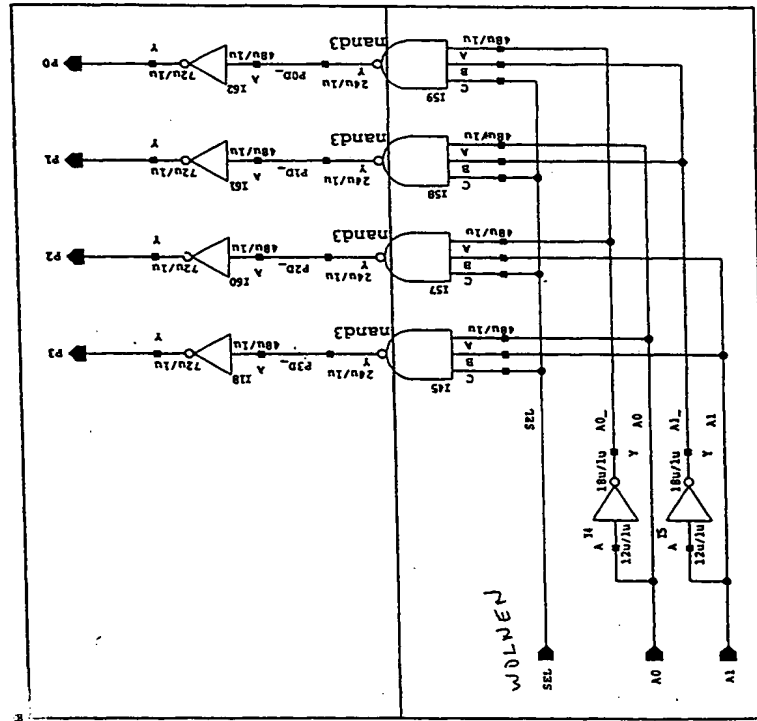
MI40-030

7.0306AA

7.0306BA

7.0306 II

FIG. 7.0306



PROJECT: L03		DESIGNER: Rotzoll	
TITLE: RRM Word Line Driver			
MADE: 103reva/ramwdr		REV: -	STD: A
DATE: Sep 29 16:04:16 1993		PART:	

**MICRON**

COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

7.0307AA	7.0307AB
7.0307BA	7.0307BB

ITEM 7.0307

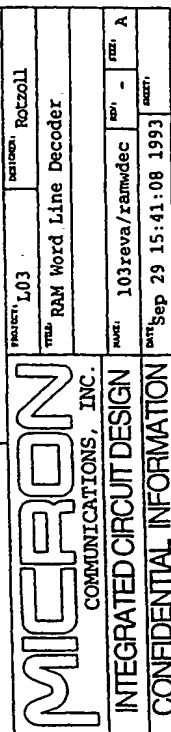


FIG. 7.0307



MI40-030

7.0308AA	7.0308AB
7.0308BA	7.0308BB

7.0308

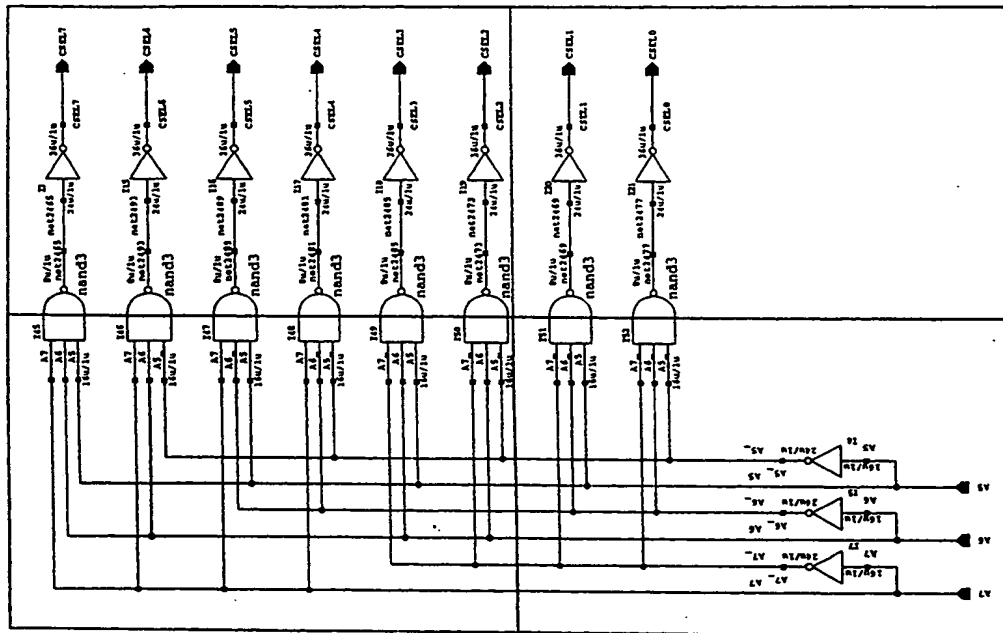


FIG. 7.0308

<b>MICRON</b> COMMUNICATIONS, INC. INTEGRATED CIRCUIT DESIGN CONFIDENTIAL INFORMATION	PART: L03 REV: 103rev0/randec DATE: Nov 5 17:21:07 1993	PROJECT: Retx011 TITLE: RAM Column Select Decode PAGE: 3 to 8 REV: - FILE: rll

7.0309AA	7.0309AB	7.0309AC	7.0309AD	7.0309AE	7.0309AF	7.0309AG
7.0309BA	7.0309BB	7.0309BC	7.0309BD	7.0309BE	7.0309BF	7.0309BG

EE 7.0309



7.0310AA	7.0310AB
7.0310BA	7.0310BB

U.S. DEPARTMENT OF JUSTICE  
FEDERAL BUREAU OF INVESTIGATION

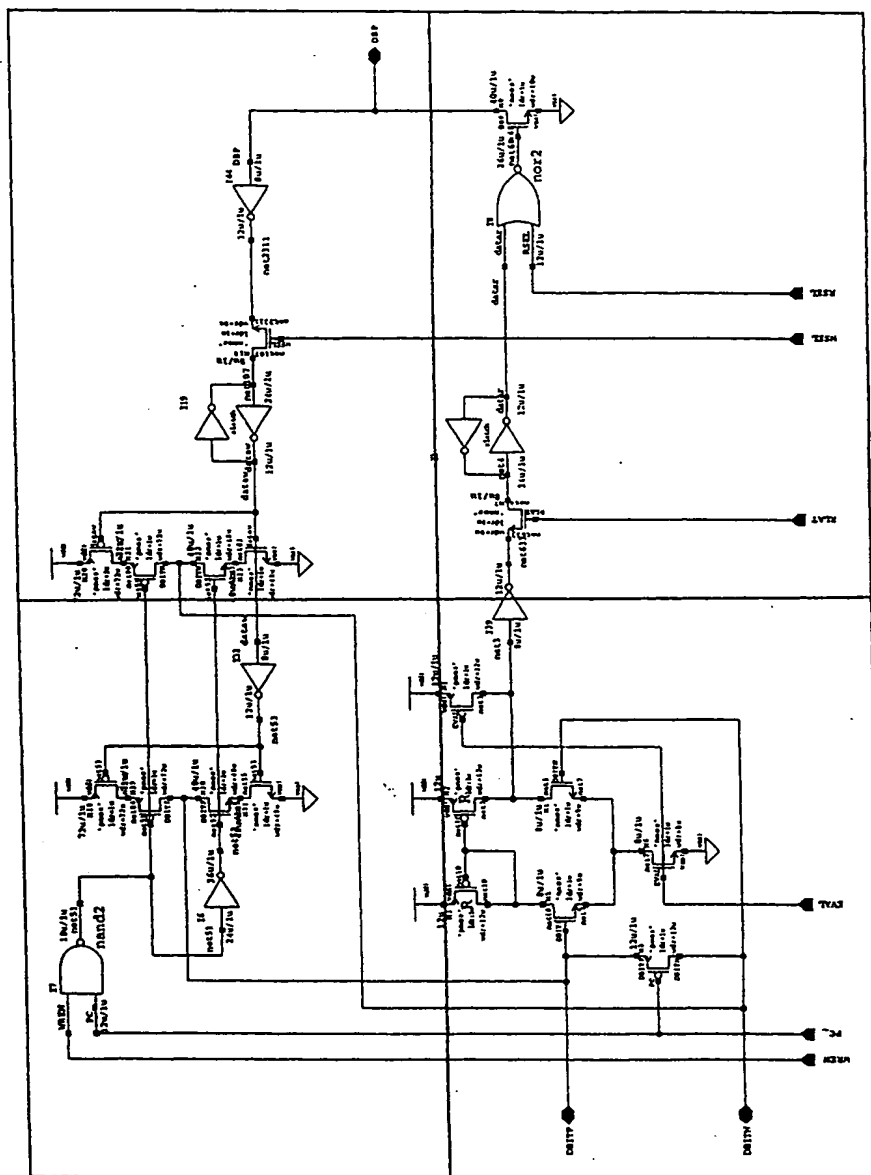


FIG. 7.0310

# NOON

COMMUNICATIONS, INC.

**INTEGRATED CIRCUIT DESIGN**

CONFIDENTIAL INFORMATION

**EXHIBIT. L03**

**Rotzoll**

RAM Databus Interface

NAME:	103reva/randb	REV: -	DATE: 11/1
-------	---------------	--------	------------

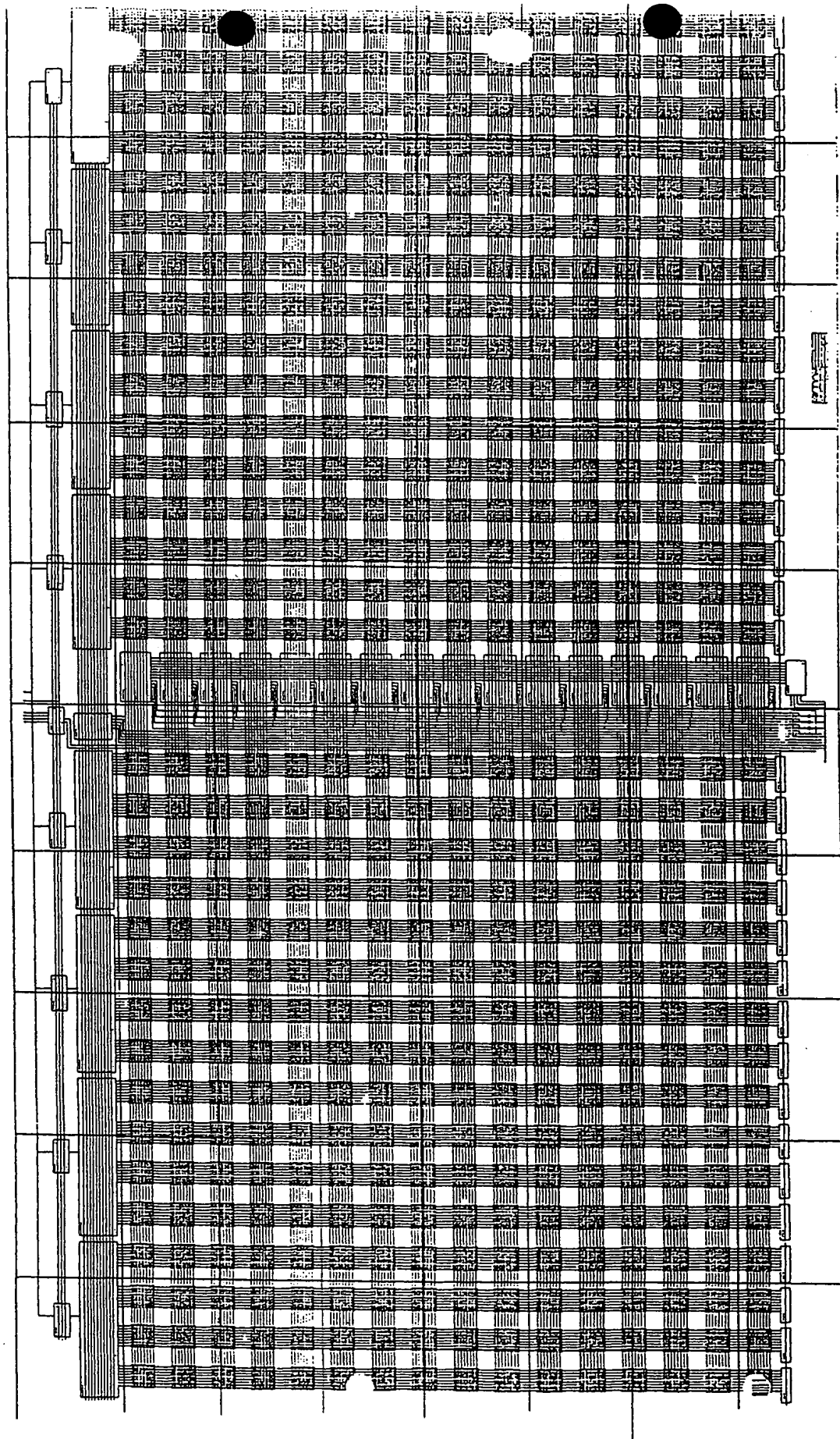
DATE: OCT 6 12:08:33 1993

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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7.04AA	7.04AB	7.04AC	7.04AD	7.04AE	7.04AF	7.04AG	7.04AH	7.04AI	7.04AJ
7.04BA	7.04BB	7.04BC	7.04BD	7.04BE	7.04BF	7.04BG	7.04BH	7.04BI	7.04BJ
7.04CA	7.04CB	7.04CC	7.04CD	7.04CE	7.04CF	7.04CG	7.04CH	7.04CI	7.04CJ
7.04DA	7.04DB	7.04DC	7.04DD	7.04DE	7.04DF	7.04DG	7.04DH	7.04DI	7.04DJ
7.04EA	7.04EB	7.04EC	7.04ED	7.04EE	7.04EF	7.04EG	7.04EH	7.04EI	7.04EJ
7.04FA	7.04FB	7.04FC	7.04FD	7.04FE	7.04FF	7.04FG	7.04FH	7.04FI	7.04FJ
7.04GA	7.04GB	7.04GC	7.04GD	7.04GE	7.04GF	7.04GG	7.04GH	7.04GI	7.04GJ
7.04HA	7.04HB	7.04HC	7.04HD	7.04HE	7.04HF	7.04HG	7.04HH	7.04HI	7.04HJ

7.0400-030

FIG. 7.04





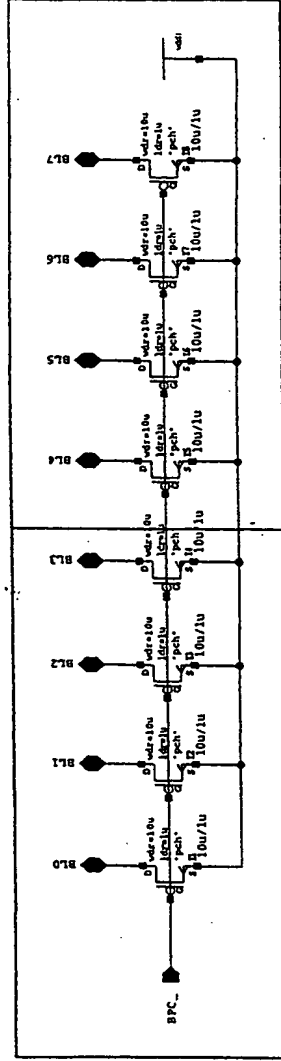
7.0401AA	7.0401AB
----------	----------

EX-11 7.0401



7.0402AA	7.0402AB
----------	----------

EE 7.0402





COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

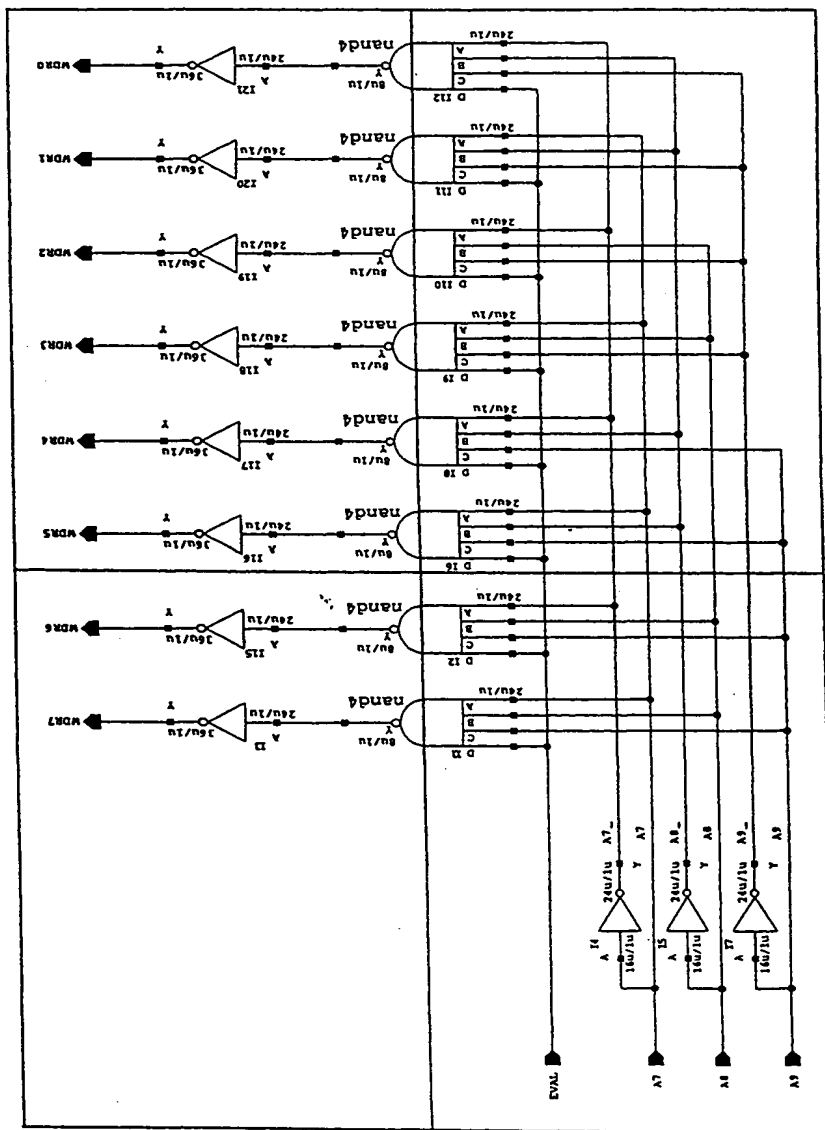
PROJECT: L03	DESIGNED: Rotzoll
TITLE: ROM Bit Line Precharge	
NAME: 103reva/rompch	REV: -
DATE: Oct 7 18:09:48 1993	SIZE: A
	SHEET: 1

Fig. 7.0902

7.0403AA	7.0403AB
7.0403BA	7.0403BB

7.0403BB

Fig. 7.0903



MICRON		PRODUCT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: ROM Word Line Driver	
INTEGRATED CIRCUIT DESIGN		DATE: 103revA/romwdr	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 7 18:11:34 1993	SHEET: A

	7.0404AB	7.0404AC
7.0404BA	7.0404BB	7.0404BC
	7.0404CB	7.0404CC
	7.0404DB	7.0404DC

II II II 7.040404

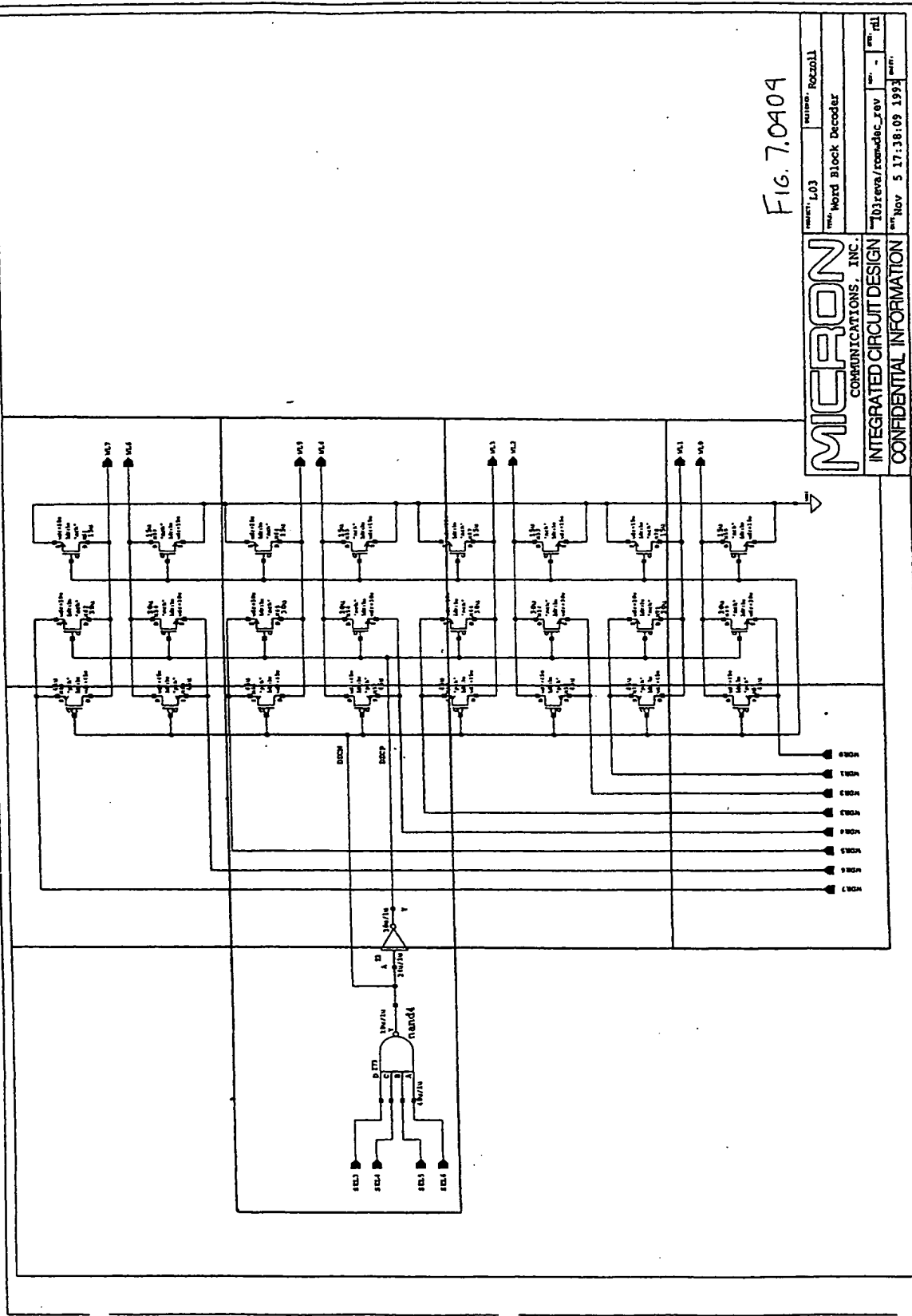


FIG. 7.0404

<b>MICRON</b> COMMUNICATIONS, INC. INTEGRATED CIRCUIT DESIGN	DESIGN: L03	DESIGN: Rev001
	NEW Word Block Decoder	
	T01rev0/romdec_rev - 5 17:38:09 1993	
CONFIDENTIAL INFORMATION		

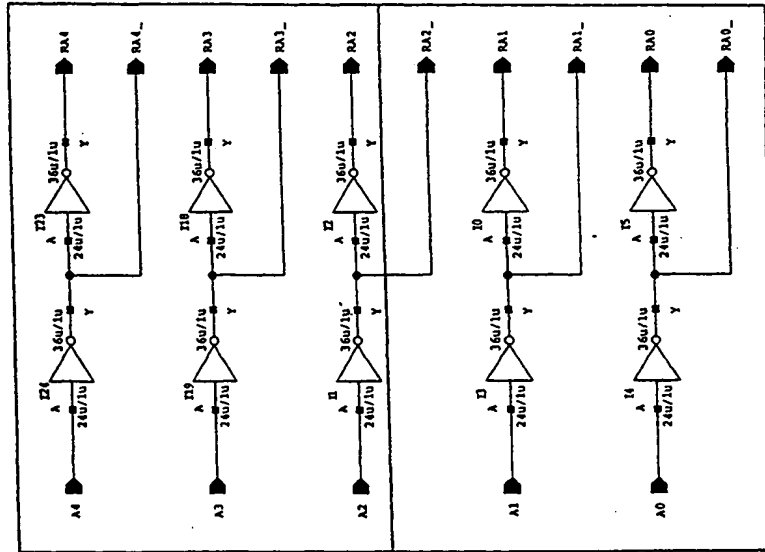


7.0405AA

7.0405BA

ISS 7.0405

Fig. 7.0405



<div>MICRON</div> <div>COMMUNICATIONS, INC.</div>				PROJECT: L03		DESIGNER: Rotzoll			
				TITLE: ROM Bit Line Address Driver					
				NUMBER: 103reva/rombldr		REV: -		CODE: A	
				DATE: Oct 7 12:08:42 1993		SHEET: 1			

**MICRON**  
COMMUNICATIONS, INC.

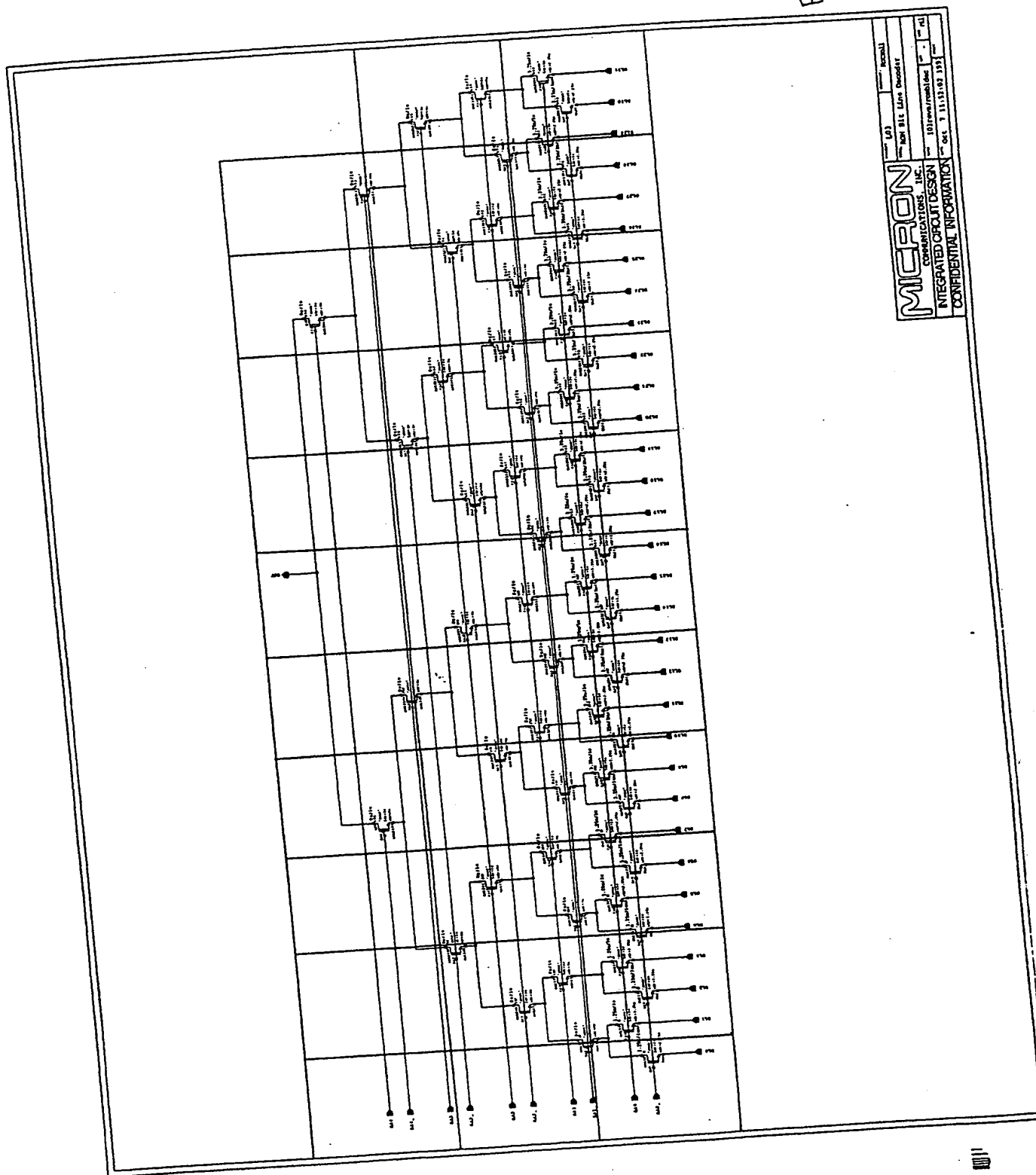
INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

7.0406AA	7.0406AB	7.0406AC	7.0406AD	7.0406AE	7.0406AF	7.0406AG	7.0406AH	7.0406AI	7.0406AJ	
7.0406BA	7.0406BB	7.0406BC	7.0406BD	7.0406BE	7.0406BF	7.0406BG	7.0406BH	7.0406BI	7.0406BJ	7.0406BK
7.0406CA	7.0406CB	7.0406CC	7.0406CD	7.0406CE	7.0406CF	7.0406CG	7.0406CH	7.0406CI	7.0406CJ	7.0406CK

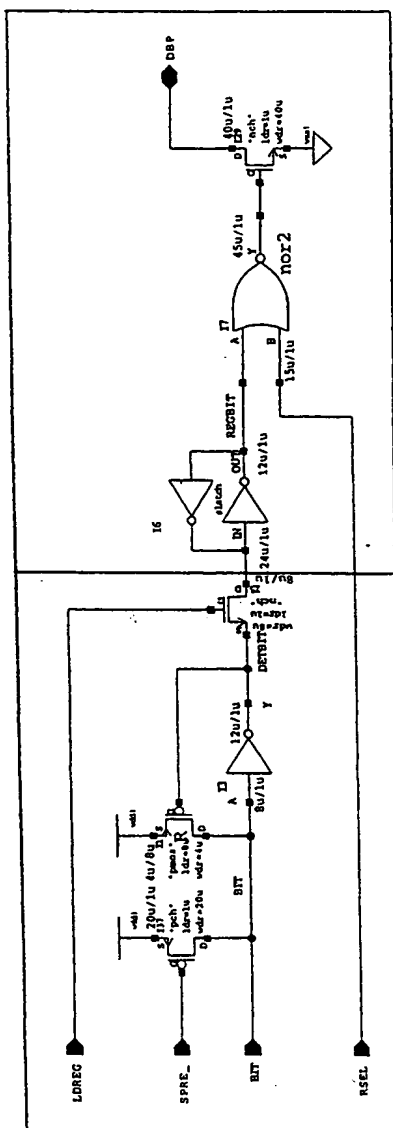
907.00.11. 1000000

FIG. 7.0406



7.0407AA	7.0407AB
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7.0407AA 7.0407AB



# 2020 COMMUNICATIONS, INC.

ROM Sense Amplifier

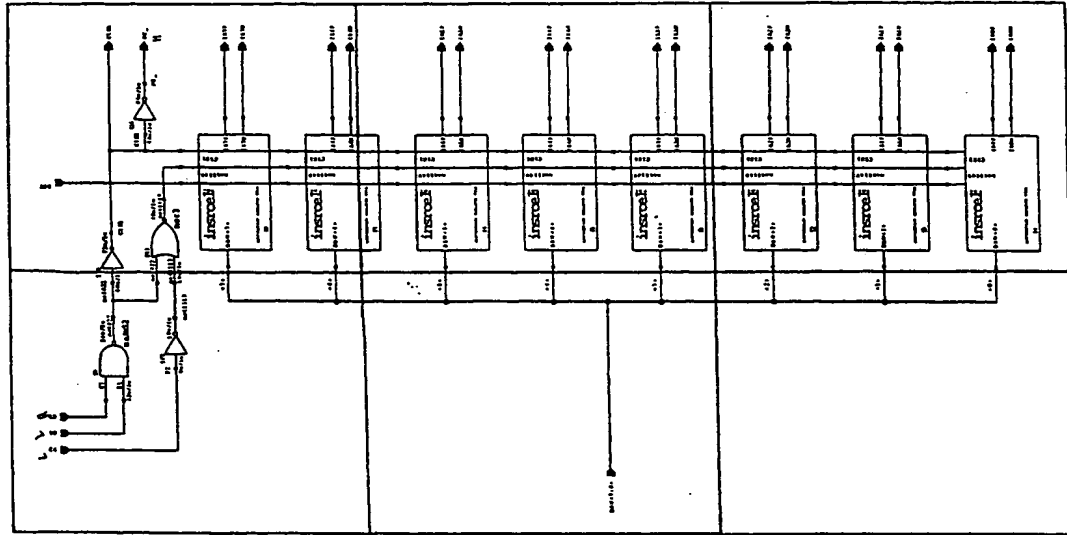
**COMMUNICATIONS, INC.**  
**INTEGRATED CIRCUIT DESIGN**

**CONFIDENTIAL INFORMATION**

7.05AA	7.05AB
7.05BA	7.05BB
7.05CA	7.05CB

Fig 7.05

Fig. 7.05

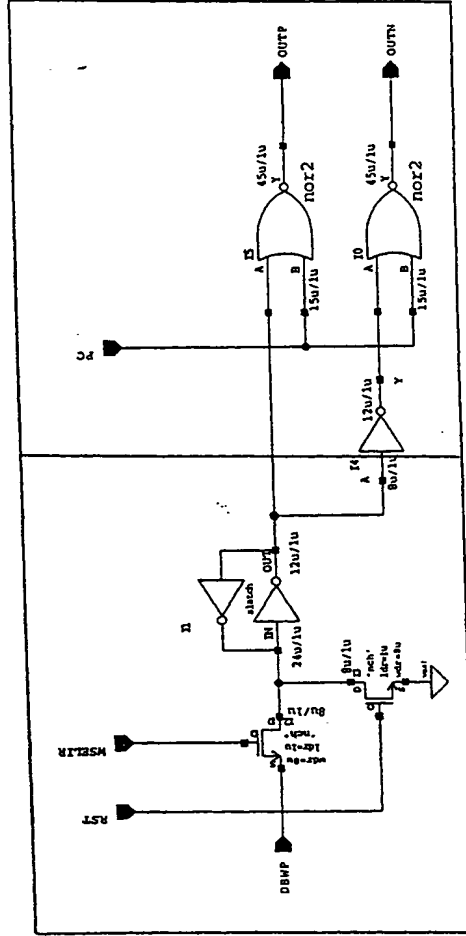




7.0501AA	7.0501AB
----------	----------

EX 7.0501

Fig. 7.0501



MICRON		PROJECT: L03	DESIGNER: Retzoll
COMMUNICATIONS, INC.		TITLE: Instruction Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/insrcel	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 5 20:12:49 1993	EXT: A

7.06AA	7.06AB	7.06AC	7.06AD	7.06AE	7.06AF	7.06AG	7.06AH	7.06AI	7.06AJ	7.06AK	7.06AL	7.06AM	7.06AN
	7.06BB	7.06BC	7.06BD	7.06BE	7.06BF	7.06BG	7.06BH	7.06BI	7.06BJ	7.06BK	7.06BL	7.06BM	7.06BN
7.06CA	7.06CB	7.06CC	7.06CD	7.06CE	7.06CF	7.06CG	7.06CH	7.06CI	7.06CJ	7.06CK	7.06CL	7.06CM	7.06CN

И. П. Т. 7.00.6

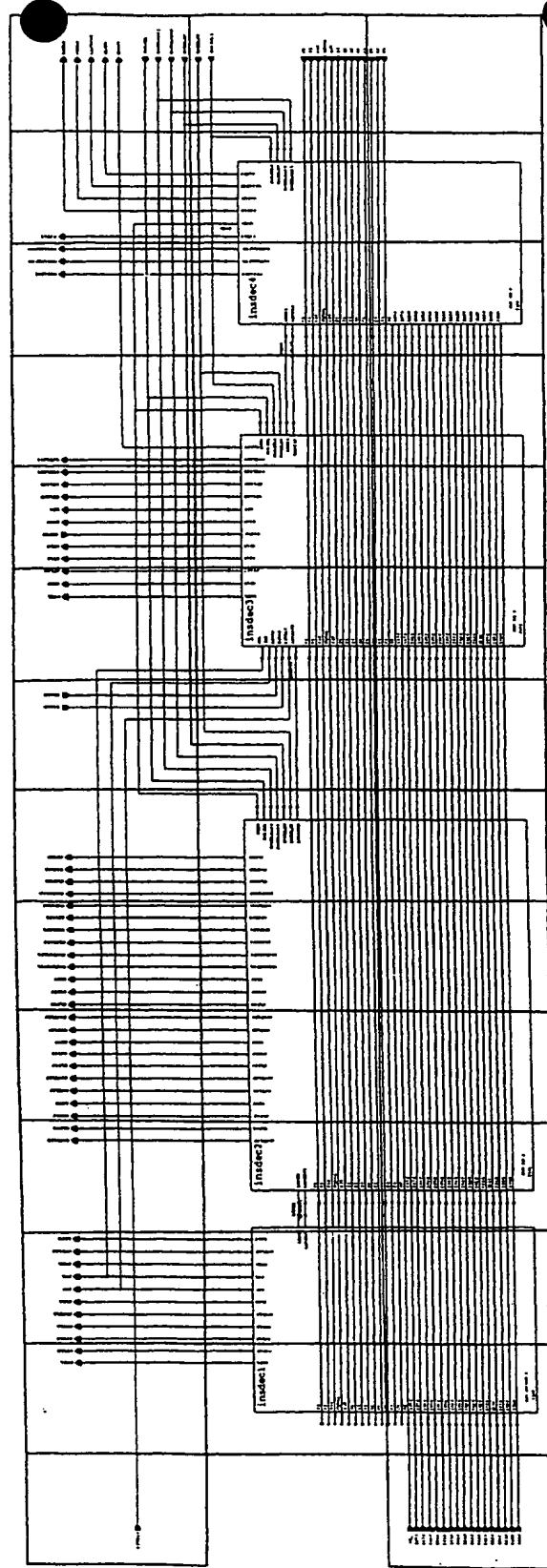


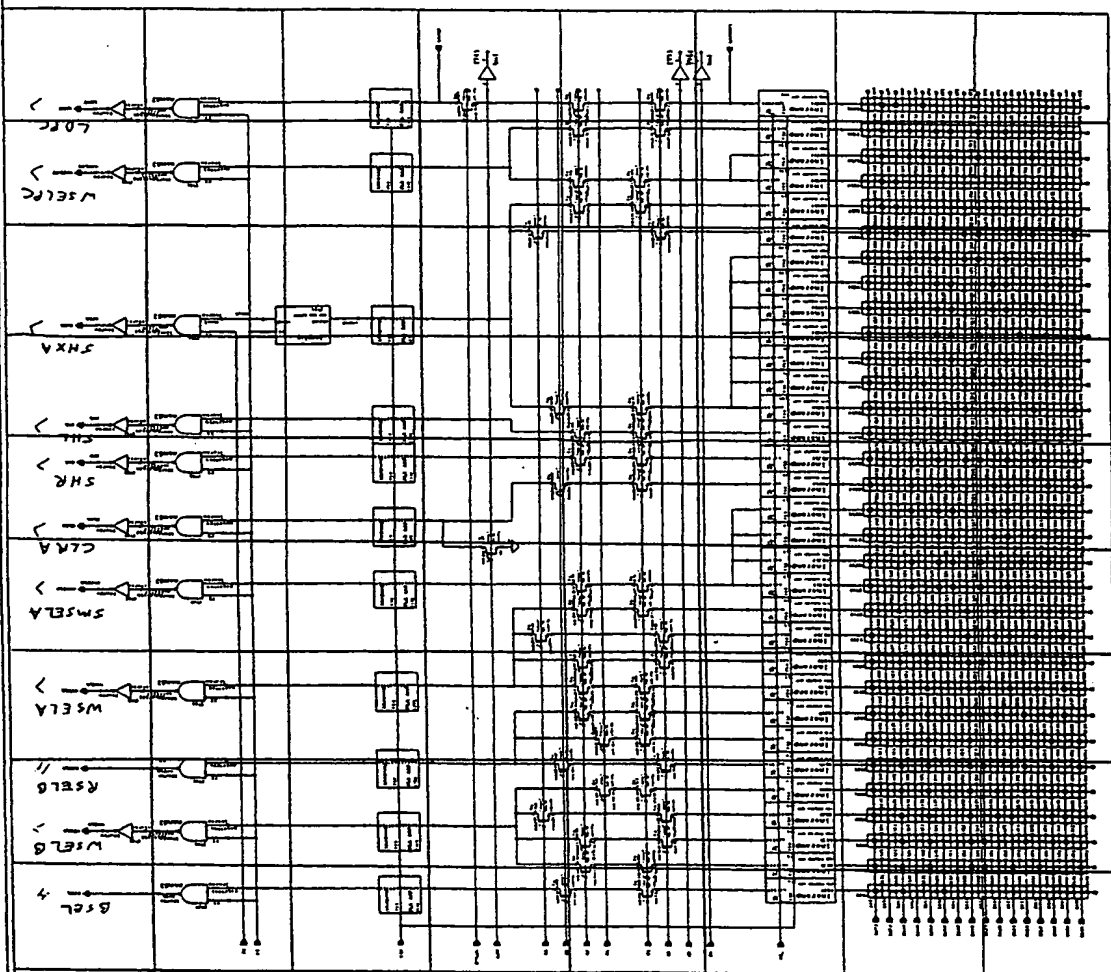
Fig. 7.06

MICRON		DATE	DESIGNED BY
INTEGRATED CIRCUIT DESIGN		REVISION	DESIGNED BY
CONSTRUCTION INFORMATION		DATE	DESIGNED BY

7.0601AA	7.0601AB	7.0601AC	7.0601AD	7.0601AE	7.0601AF	7.0601AG	7.0601AH	7.0601AI
7.0601BA	7.0601BB	7.0601BC	7.0601BD	7.0601BE	7.0601BF	7.0601BG	7.0601BH	7.0601BI
7.0601CA	7.0601CB	7.0601CC	7.0601CD	7.0601CE	7.0601CF	7.0601CG	7.0601CH	7.0601CI
7.0601DA	7.0601DB	7.0601DC	7.0601DD	7.0601DE	7.0601DF	7.0601DG	7.0601DH	7.0601DI
7.0601EA	7.0601EB	7.0601EC	7.0601ED	7.0601EE	7.0601EF	7.0601EG	7.0601EH	7.0601EI
7.0601FA	7.0601FB	7.0601FC	7.0601FD	7.0601FE	7.0601FF	7.0601FG	7.0601FH	7.0601FI
7.0601GA	7.0601GB	7.0601GC	7.0601GD	7.0601GE	7.0601GF	7.0601GG	7.0601GH	7.0601GI
7.0601HA	7.0601HB	7.0601HC	7.0601HD	7.0601HE	7.0601HF	7.0601HG	7.0601HH	7.0601HI

II II II 7.0601 II

FIG. 7.0601



7.0602AA	7.0602AB	7.0602AC	7.0602AD	7.0602AE	7.0602AF	7.0602AG	7.0602AH
7.0602BA	7.0602BB	7.0602BC	7.0602BD	7.0602BE	7.0602BF	7.0602BG	7.0602BH
7.0602CA	7.0602CB	7.0602CC	7.0602CD	7.0602CE	7.0602CF	7.0602CG	7.0602CH
7.0602DA	7.0602DB	7.0602DC	7.0602DD	7.0602DE	7.0602DF	7.0602DG	7.0602DH
7.0602EA	7.0602EB	7.0602EC	7.0602ED	7.0602EE	7.0602EF	7.0602EG	7.0602EH
7.0602FA	7.0602FB	7.0602FC	7.0602FD	7.0602FE	7.0602FF	7.0602FG	7.0602FH
7.0602GA	7.0602GB	7.0602GC	7.0602GD	7.0602GE	7.0602GF	7.0602GG	7.0602GH
7.0602HA	7.0602HB	7.0602HC	7.0602HD	7.0602HE	7.0602HF	7.0602HG	7.0602HH
		7.0602IC	7.0602ID	7.0602IE	7.0602IF	7.0602IG	7.0602IH
		7.0602JC	7.0602JD	7.0602JE	7.0602JF	7.0602JG	7.0602JH

7.0602

Fig. 7.0602



7.0603AA	7.0603AB	7.0603AC	7.0603AD	7.0603AE	7.0603AF	7.0603AH	7.0603AI	7.0603AJ
7.0603BA	7.0603BB	7.0603BC	7.0603BD	7.0603BE	7.0603BF	7.0603BG	7.0603BI	7.0603BJ
7.0603CA	7.0603CB	7.0603CC	7.0603CD	7.0603CE	7.0603CF	7.0603CG	7.0603CI	7.0603CJ
7.0603DA	7.0603DB	7.0603DC	7.0603DD	7.0603DE	7.0603DF	7.0603DG	7.0603DI	7.0603DJ
7.0603EA	7.0603EB	7.0603EC	7.0603ED	7.0603EE	7.0603EF	7.0603EG	7.0603EI	7.0603EJ
7.0603FA	7.0603FB	7.0603FC	7.0603FD	7.0603FE	7.0603FF	7.0603FG	7.0603FI	7.0603FJ
7.0603GA	7.0603GB	7.0603GC	7.0603GD	7.0603GE	7.0603GF	7.0603GG	7.0603GI	7.0603GJ
7.0603HA	7.0603HB	7.0603HC	7.0603HD	7.0603HE	7.0603HF	7.0603HG	7.0603HI	7.0603HJ
7.0603IA	7.0603IB	7.0603IC	7.0603ID	7.0603IE	7.0603IF	7.0603IG	7.0603IH	7.0603IJ
		7.0603JC	7.0603JD	7.0603JE	7.0603JF	7.0603JG	7.0603JI	
								7.0603BK


 DEPARTMENT OF DEFENSE

DATE	00-0-00
BY	00-0-00
FOR	00-0-00
REVISION	00-0-00
DESCRIPTION	00-0-00

00-0-00

CBC clear carry

pin 6A

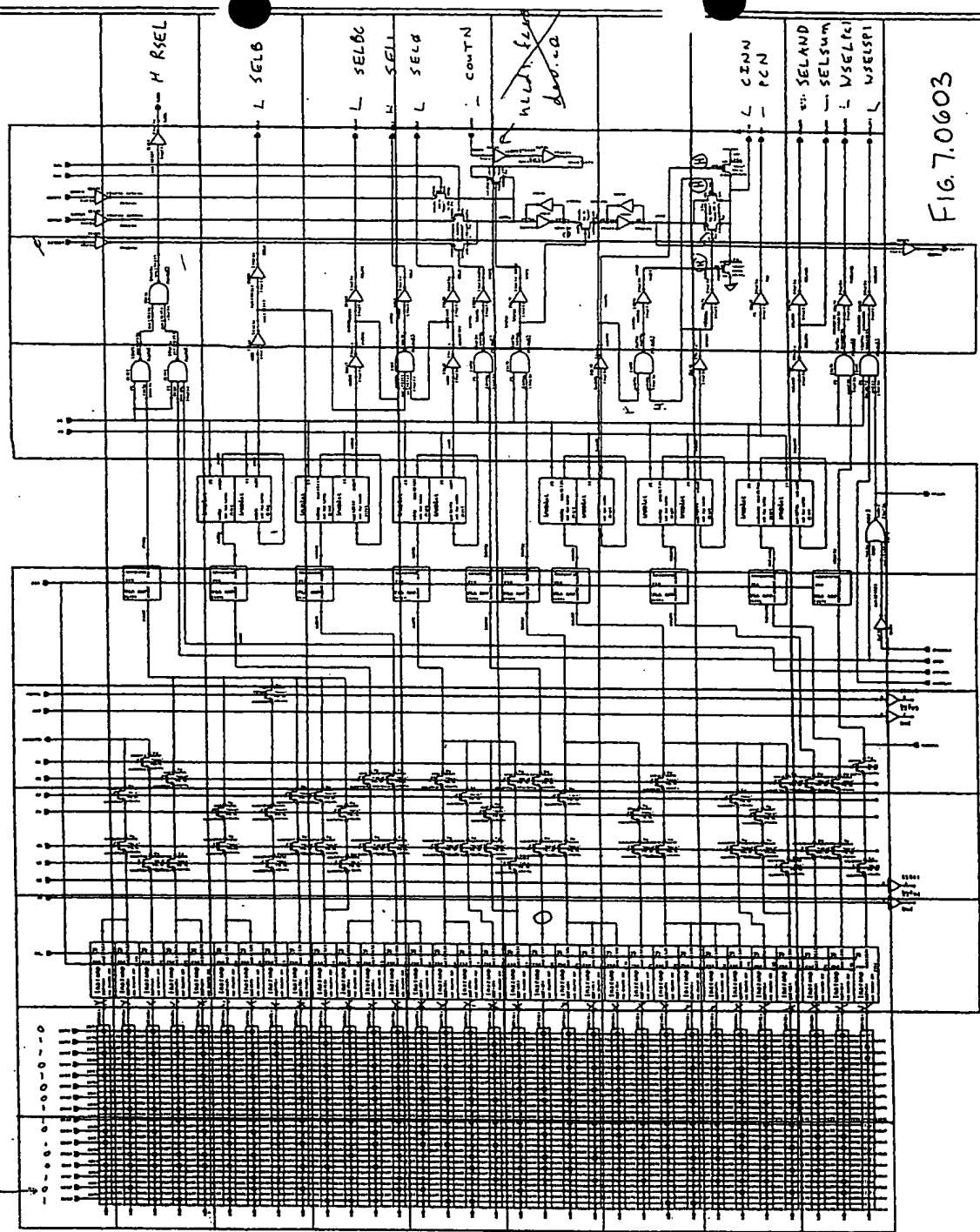


FIG. 7.0603

7.0604AA	7.0604AB	7.0604AC	7.0604AD	7.0604AE	7.0604AF	7.0604AG	7.0604AH	7.0604AI
7.0604BA	7.0604BB	7.0604BC	7.0604BD	7.0604BE	7.0604BF	7.0604BG	7.0604BH	7.0604BI
7.0604CA	7.0604CB	7.0604CC	7.0604CD	7.0604CE	7.0604CF	7.0604CG	7.0604CH	7.0604CI
7.0604DA	7.0604DB	7.0604DC	7.0604DD	7.0604DE	7.0604DF	7.0604DG	7.0604DH	7.0604DI
7.0604EA	7.0604EB	7.0604EC	7.0604ED	7.0604EE	7.0604EF	7.0604EG	7.0604EH	7.0604EI
7.0604FA	7.0604FB	7.0604FC	7.0604FD	7.0604FE	7.0604FF	7.0604FG	7.0604FH	7.0604FI
7.0604GA	7.0604GB	7.0604GC	7.0604GD	7.0604GE	7.0604GF	7.0604GG	7.0604GH	7.0604GI
7.0604HA	7.0604HB	7.0604HC	7.0604HD	7.0604HE	7.0604HF	7.0604HG		
7.0604IA	7.0604IB	7.0604IC	7.0604ID	7.0604IE	7.0604IF	7.0604IG		
7.0604JA	7.0604JB	7.0604JC	7.0604JD	7.0604JE	7.0604JF	7.0604JG	7.0604JH	7.0604JI

7.0604

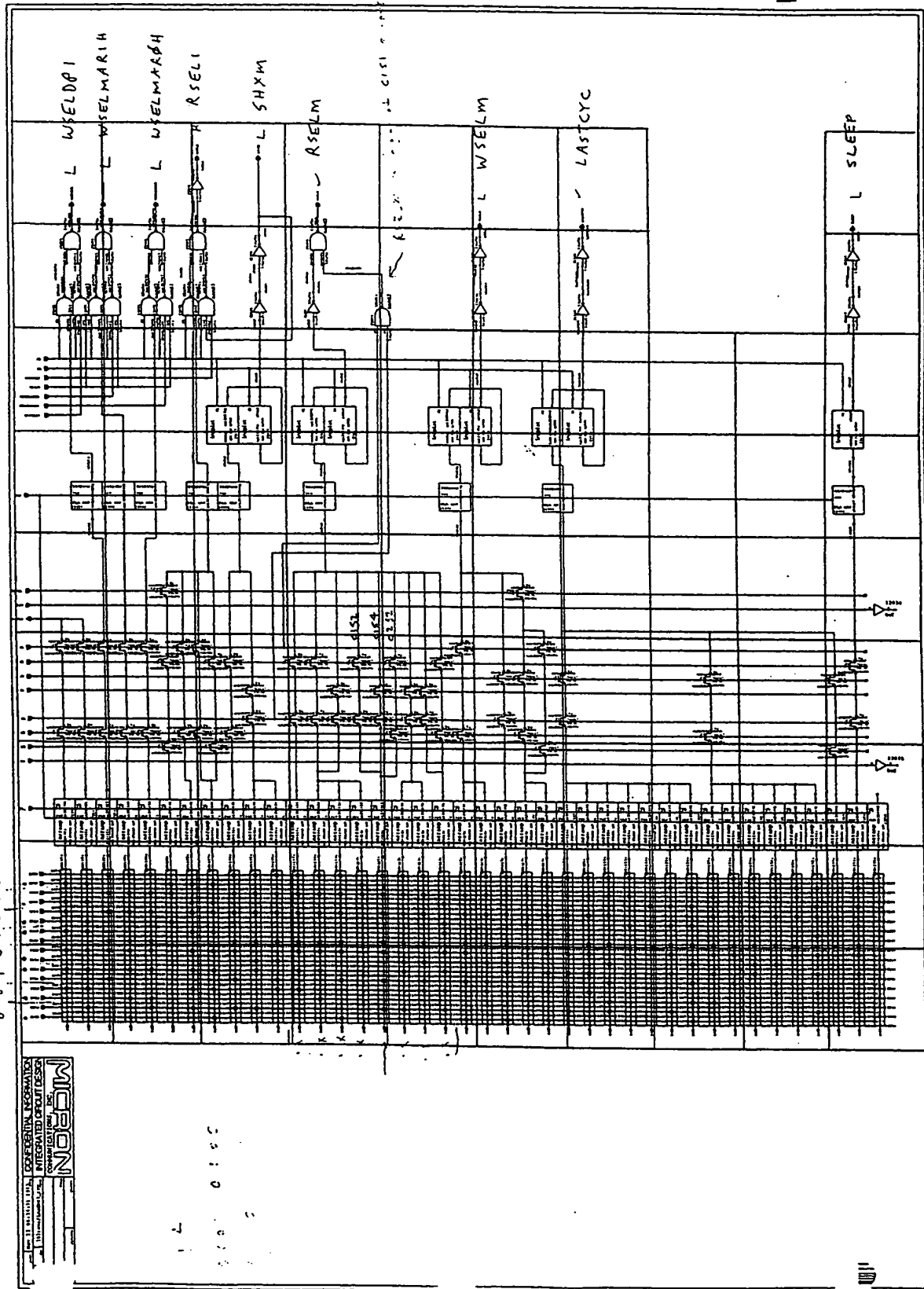


FIG. 7.06



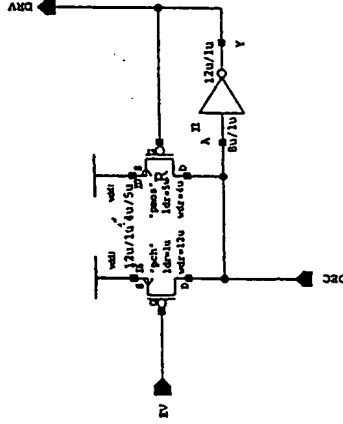


Fig. 7.060402

MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: Instruction Decoder PLA Amp	
INTEGRATED CIRCUIT DESIGN		MODEL: 103reva/inspamp	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 6 12:21:34 1993	SIZE: A

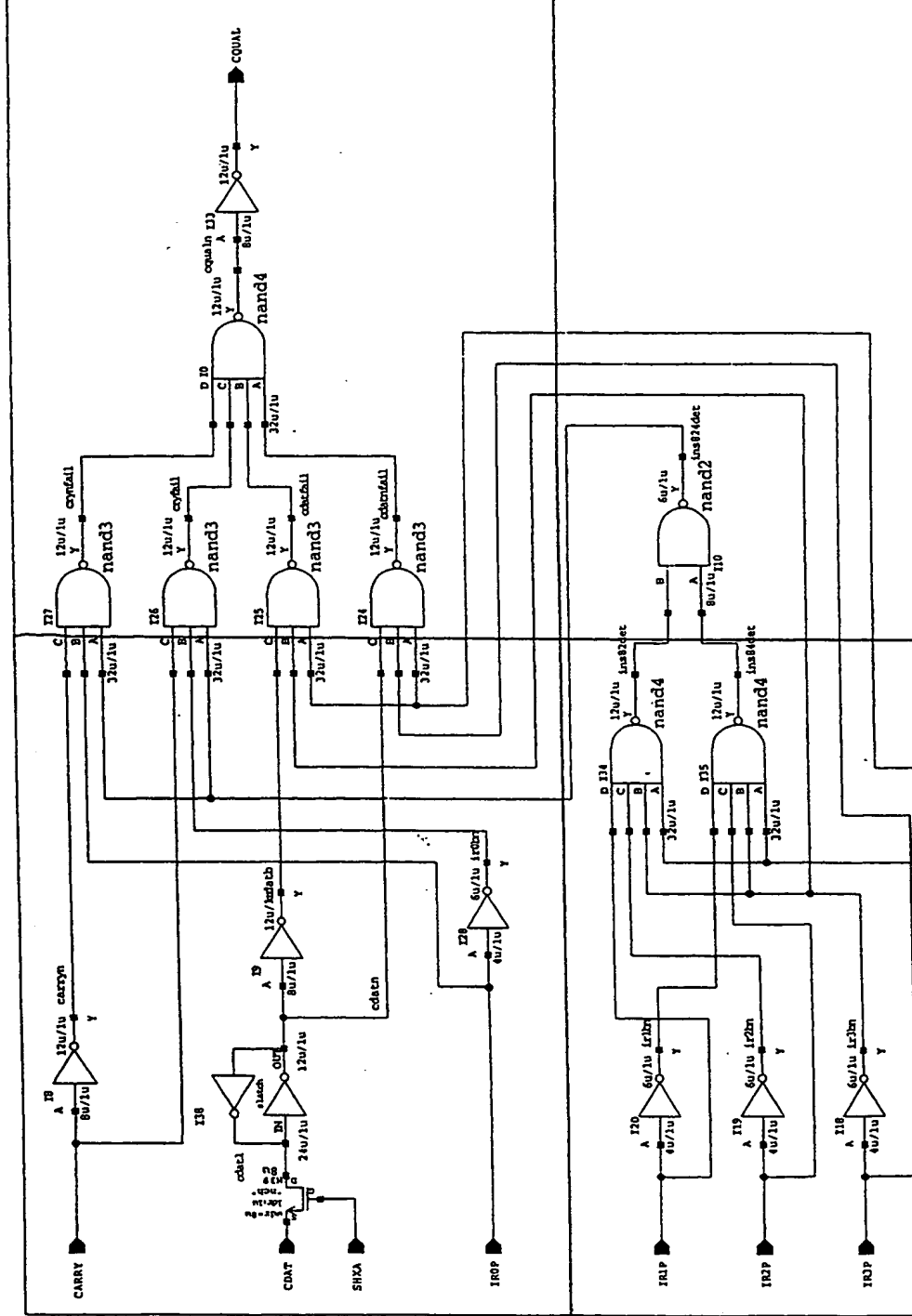


7.07AA	7.07AB
7.07BA	7.07BB

EX-107



Fig. 7.07



<b>MICRON</b>		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: Conditional Qualifier Decoder	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/cqualdec	REV: -
CONFIDENTIAL INFORMATION		DATE: Nov 17 20:09:12 1993	USER: A

7.08AA

7.08BA

7.08CA

7.08 7.08B

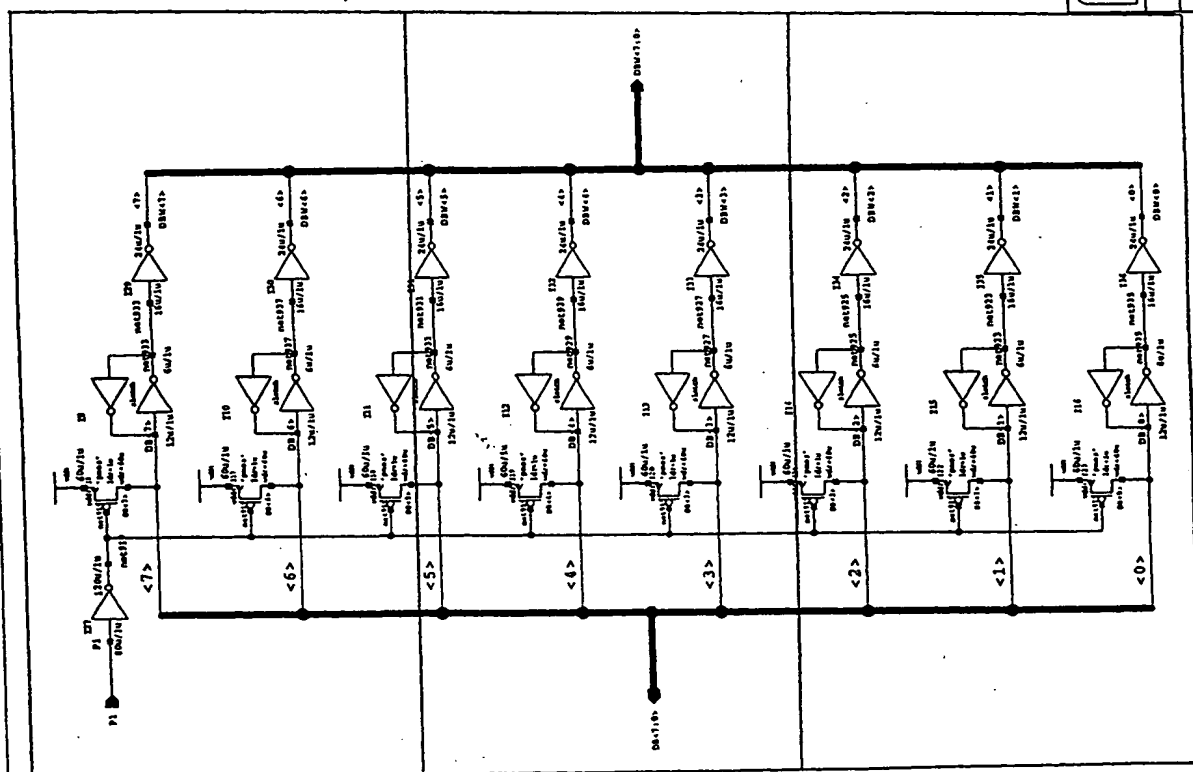


Fig. 7.08

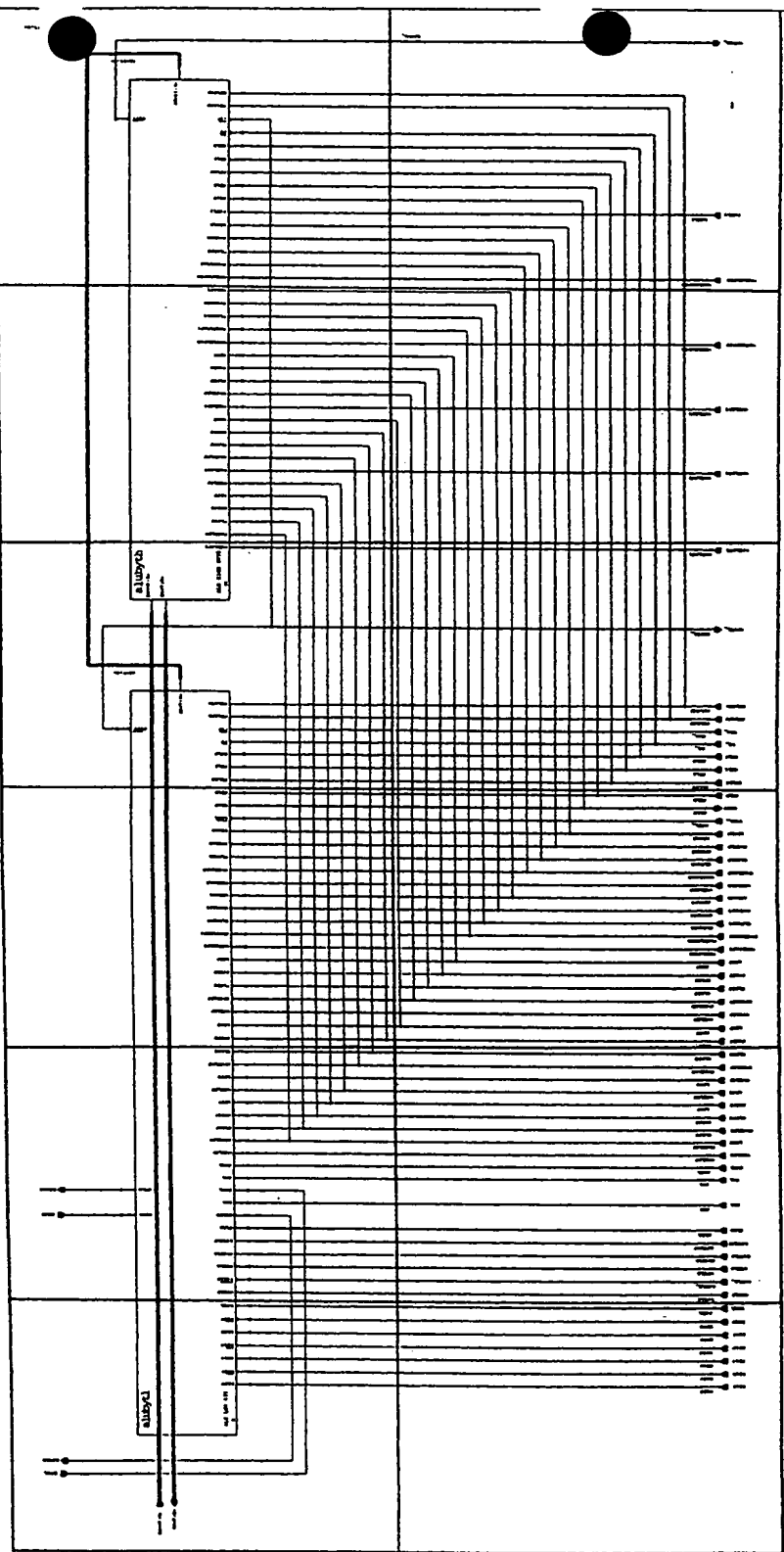
MICRON		PRODUCT: L03	REVISION: Rev2.01
COMMUNICATIONS, INC.		NAME: Databus Latch/Precharge	
INTEGRATED CIRCUIT DESIGN		DATE: 10/27/84	BY: J. J. J.
CONFIDENTIAL INFORMATION		DATE: Oct 1 14:51:49 1993	REV: 1

7.09AA	7.09AB	7.09AC	7.09AD	7.09AE	7.09AF
7.09BA	7.09BB	7.09BC	7.09BD	7.09BE	7.09BF

EX-7.09

Fig. 7.09

**MICRON**  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION



7.0901AA	7.0901AB	7.0901AC	7.0901AD	7.0901AE
7.0901BA	7.0901BB	7.0901BC	7.0901BD	7.0901BE
7.0901CA	7.0901CB	7.0901CC	7.0901CD	7.0901CE

II II II II II II II II

Fig. 7.0901

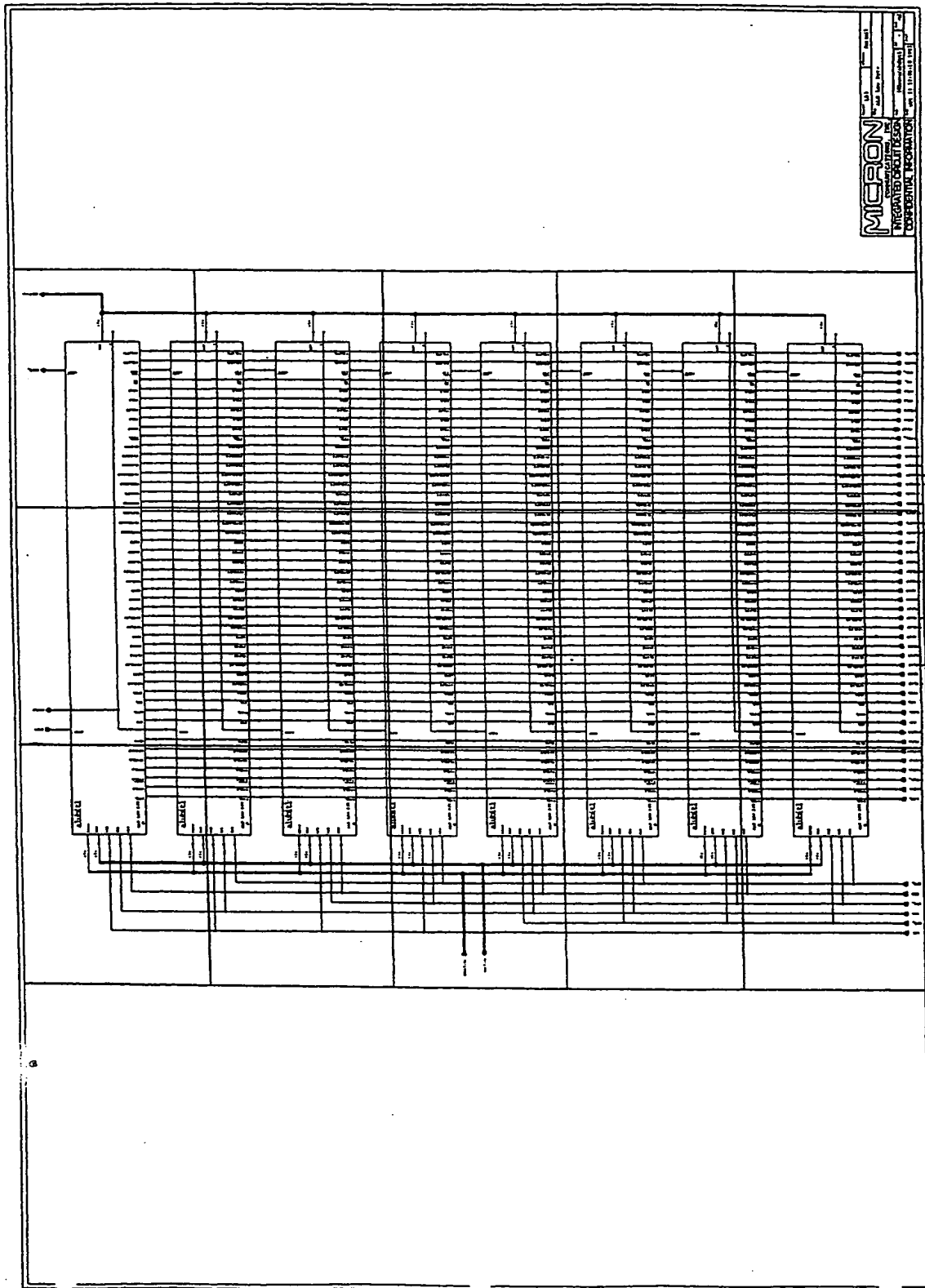
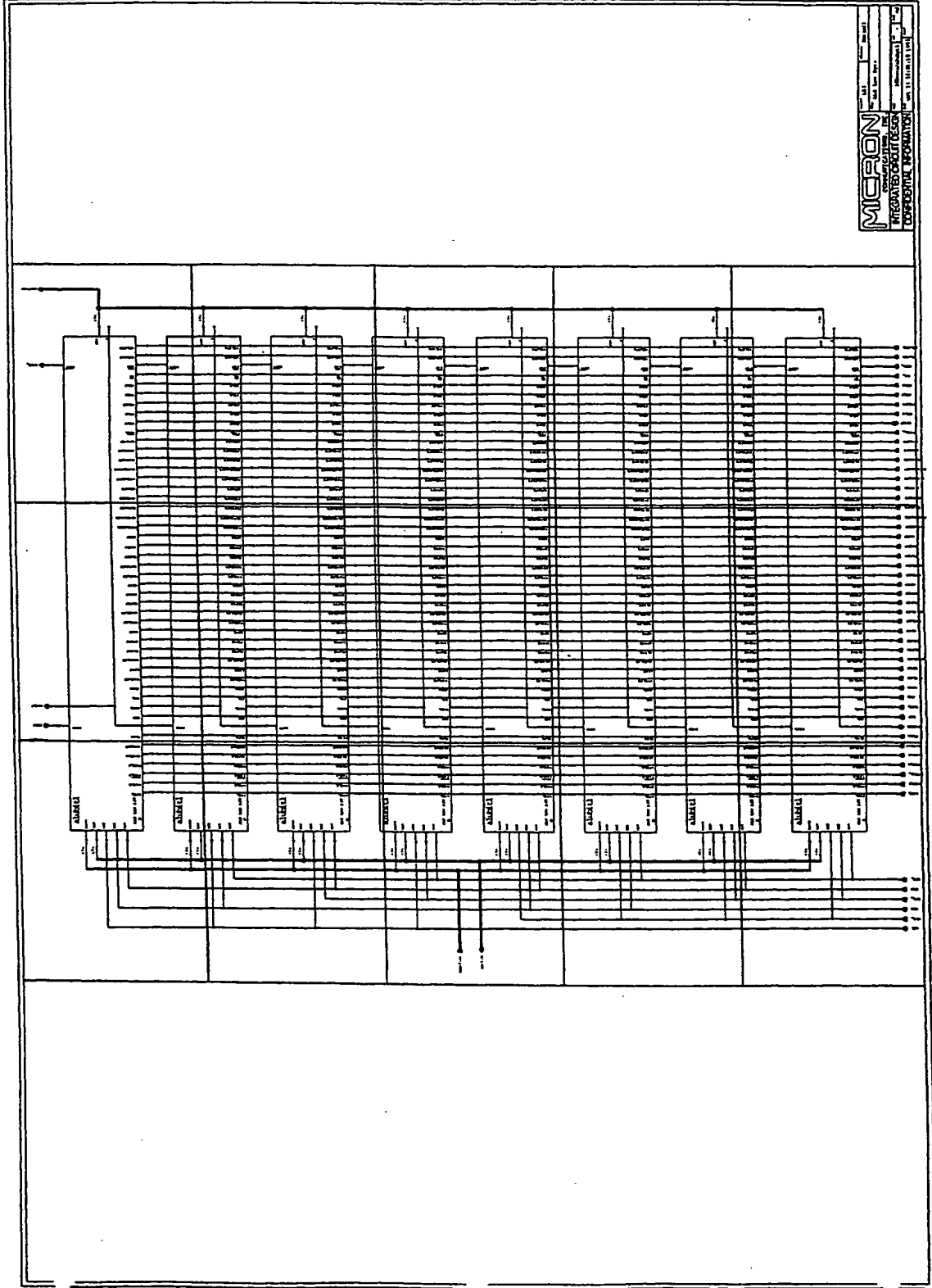


FIG. 7.0901





7.090101AA	7.090101AB	7.090101AC	7.090101AD
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II II II II II II II II II II







7.09010103AA	7.09010103AB
--------------	--------------

7.09010103AA

ENTRADA

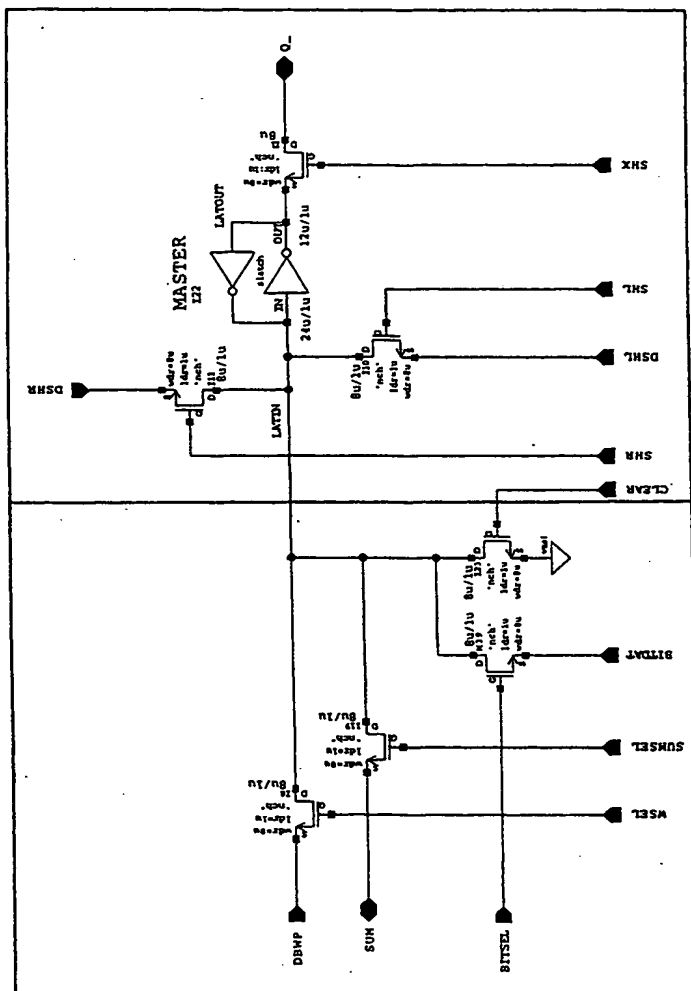


FIG. 7.09010103

PROJECT: L03		DESIGNER: Rotzoll
TITLE: ALU A Register Cell		
PROJECT: 103revA/aluacell	REV: -	ITER: A
DATE: Oct 1 15:41:37 1993		SHEET:

7.09010104AA	7.09010104AB
--------------	--------------

II II 7.09010104

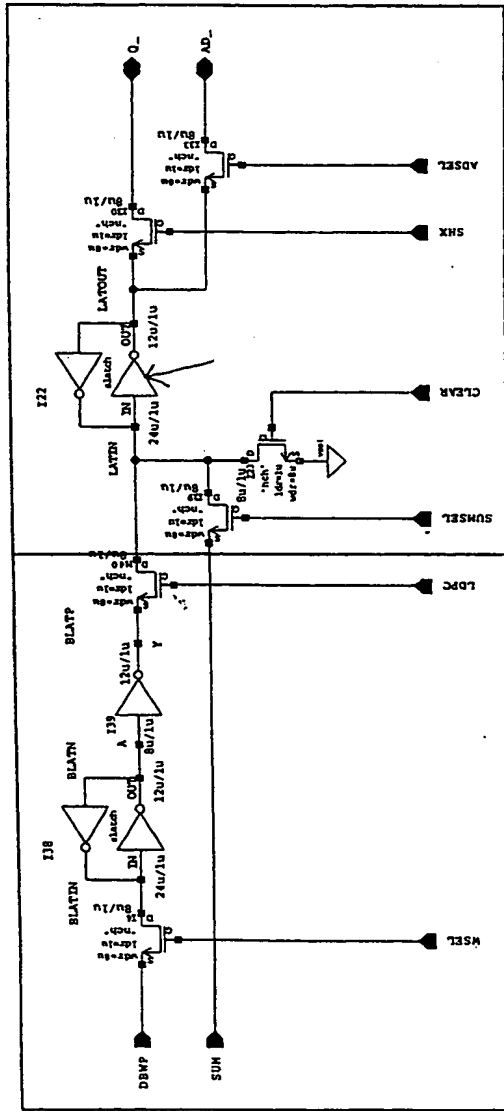
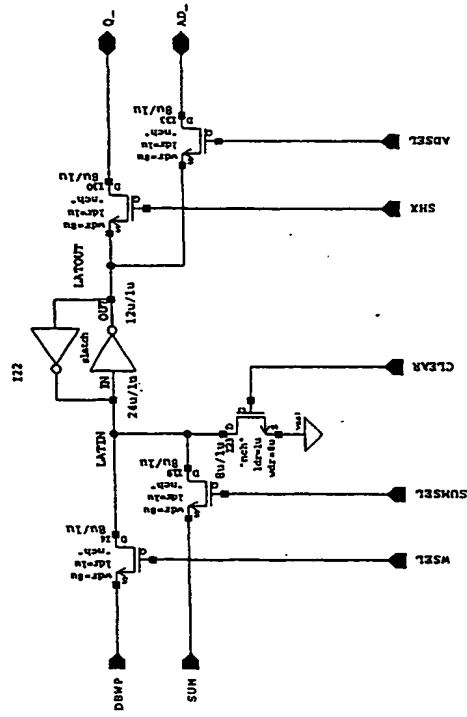


Fig. 7.09010104

<div>MICRON</div> <div>COMMUNICATIONS, INC.</div>				PROJECT: L03		DESIGNER: Rotzoll	
				TITLE: ALU Register Cell			
				NAME:	103reva/alupc	REV: -	EXES: A
				DATE:	Oct 1 15:45:48 1993		
						SHEET:	
INTEGRATED CIRCUIT DESIGN							
CONFIDENTIAL INFORMATION							



Fig. 7.09010105



MICRON		PROJECT: L03	DESIGN: Rotzoll
COMMUNICATIONS, INC.		TITLE: ALU Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/alurcell	REV: -
CONFIDENTIAL INFORMATION		DATE: Oct 1 15:51:03 1993	SHEET: A

7.09010106AA	7.09010106AB
--------------	--------------

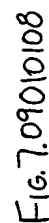
EX 7.09010106





7.09010108AA	7.09010108AB	7.09010108AC
7.09010108BA	7.09010108BB	7.09010108BC

BRITANNIA



**B85: move feedback device from I21 to I27**

**JOTOOLE**

NAVJAG, LOS

**micron**  
COMMUNICATIONS, INC.

## INTEGRATED CIRCUIT DESIGN

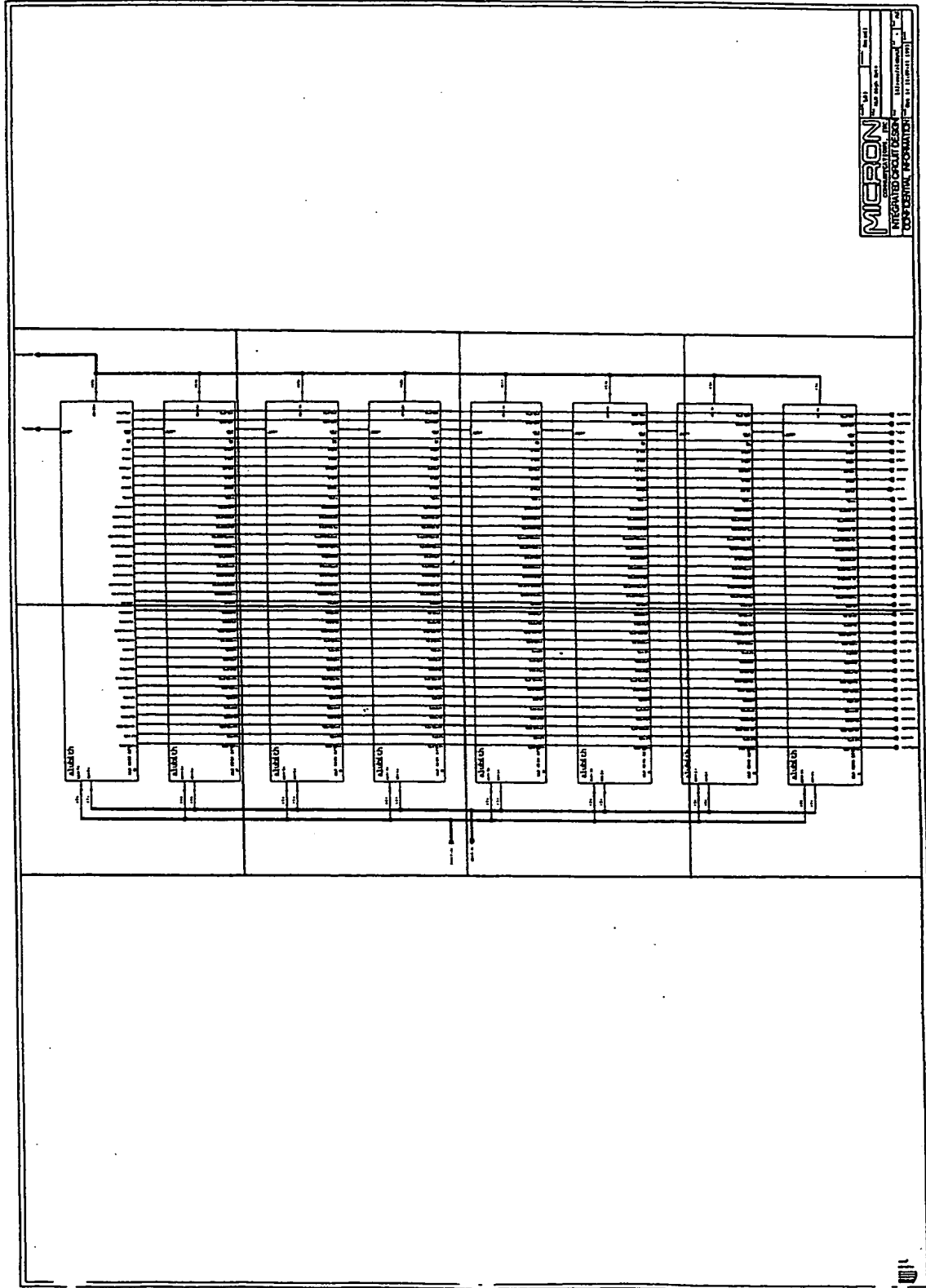
**CONFIDENTIAL INFORMATION**

1336

7.0902AA	7.0902AB	7.0902AC	7.0902AD
7.0902BA	7.0902BB	7.0902BC	7.0902BD

EX 1.0902

Fig. 7.0902





7.090201AA	7.090201AB	7.090201AC
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EX 7.090201

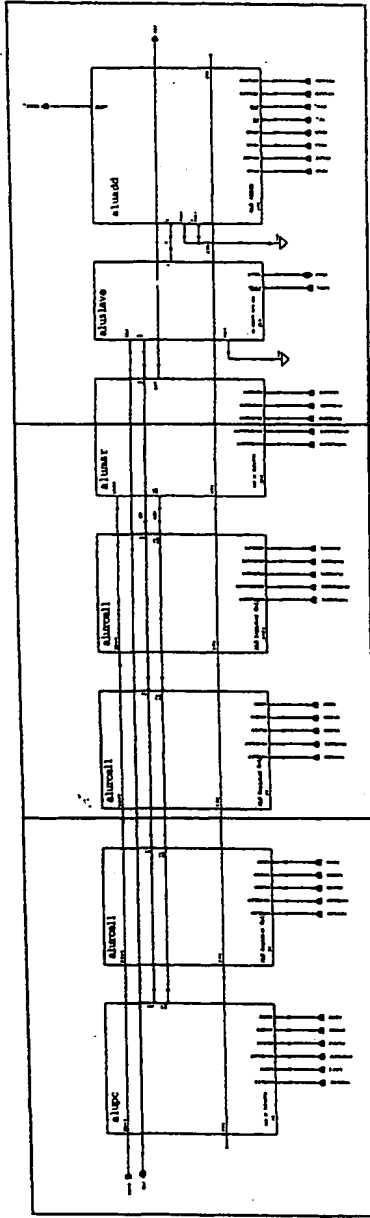
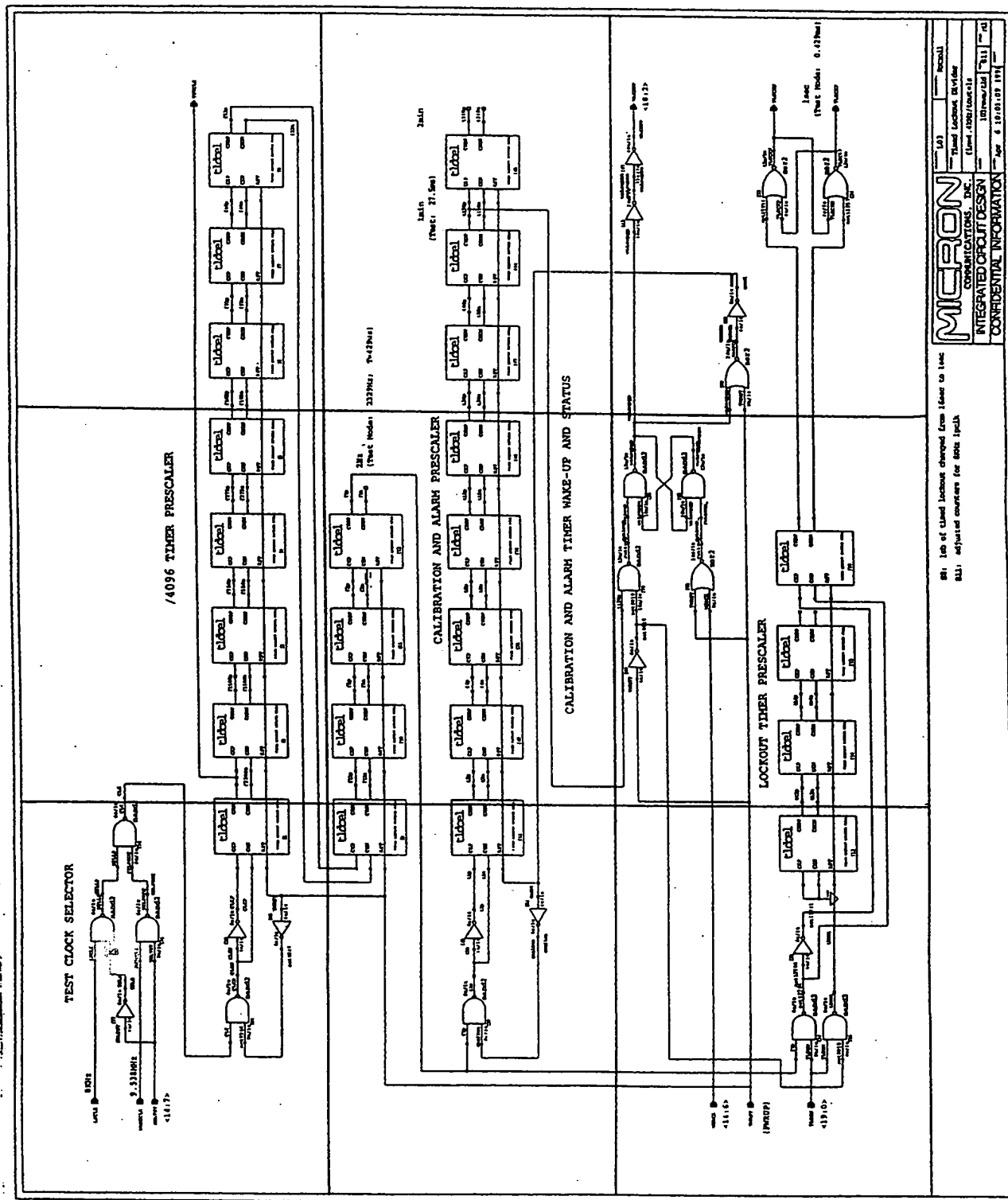


FIG. 7.090201

7.10AA	7.10AB	7.10AC
7.10BA	7.10BB	7.10BC
7.10CA	7.10CB	7.10CC

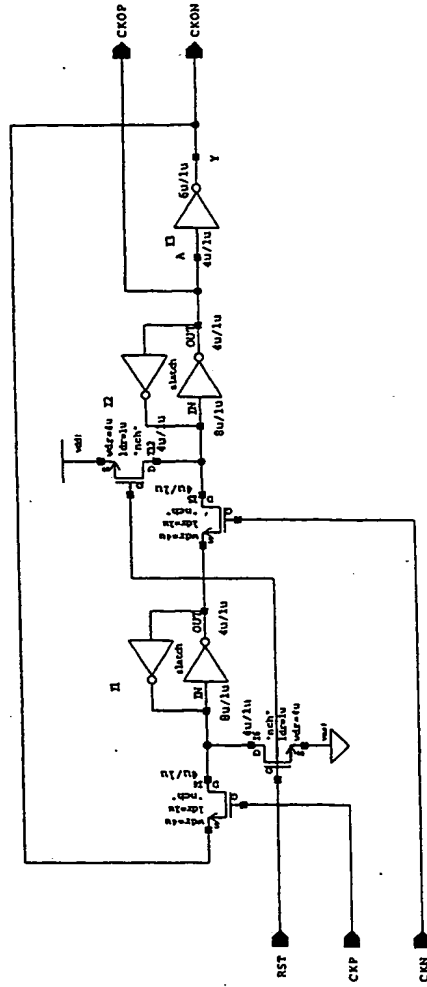
II. II. II. II.

FIG. 7.10



**MICRON**  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION  
 Doc. 6 10101010 1010

81. Lab of clock lockout changed from 100ns to 10ns  
 81.1. adjusted counters for 10ns input



12/29/92

<b>MICRON</b>				DESIGNER: Rotzoll	
COMMUNICATIONS, INC.				TITLE: Timed Lockout Divider Cell	
INTEGRATED CIRCUIT DESIGN				NUMBER: 103revA/tdlcel	SIZE: A
CONFIDENTIAL INFORMATION				DATE: Sep 22 15:26:56 1994	SHEET: 1

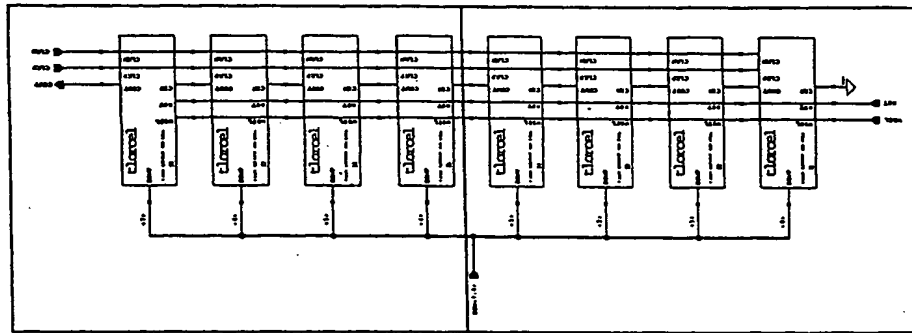
**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

Fig. 7.1001

7.11AA	7.11AB
--------	--------

Exhibit 7.11

FIG. 7.11

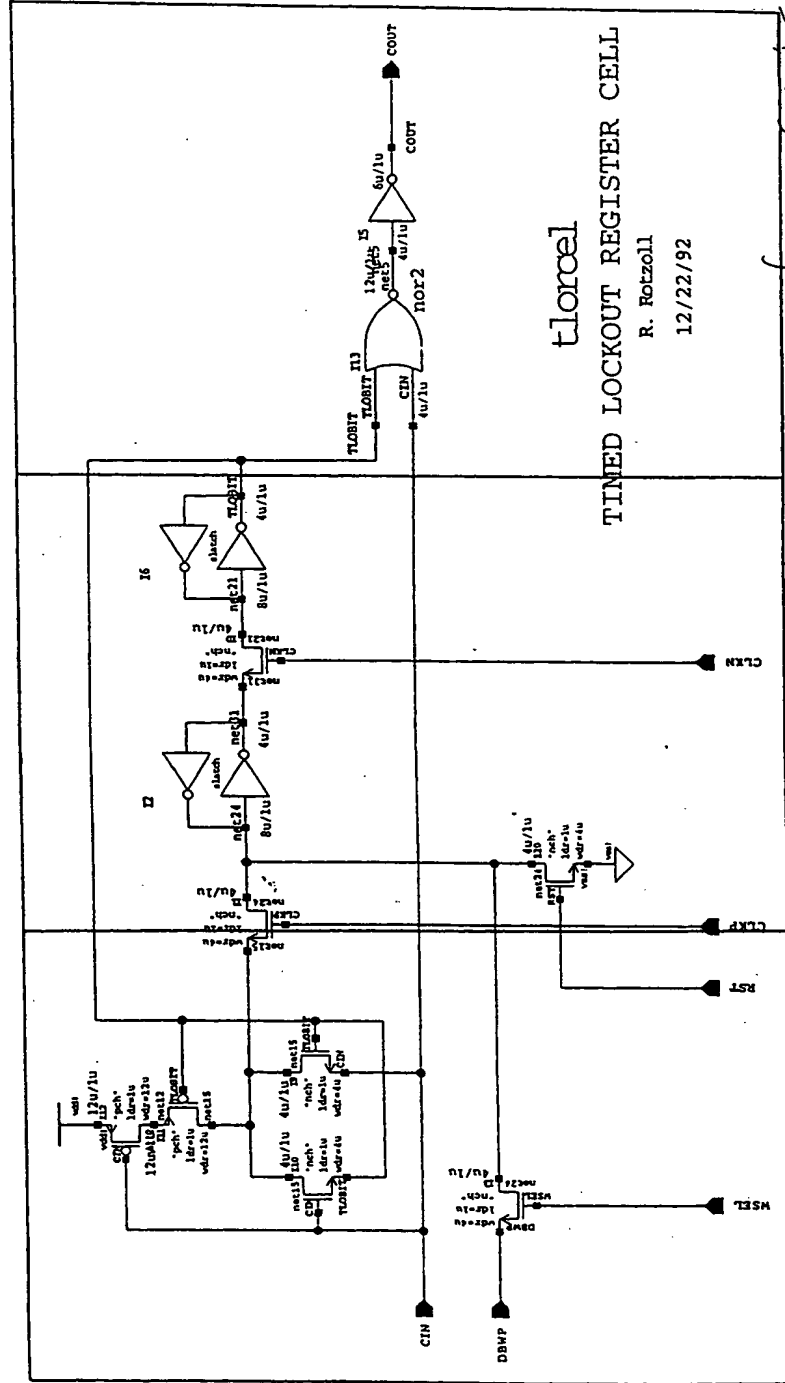


<b>MICRON</b>		103	Recess
COMMUNICATIONS, INC.		Transit Lockout Amplifier	
INTEGRATED CIRCUIT DESIGN		103	Recess
CONFIDENTIAL INFORMATION		Oct 1 11 05:17 1991	103

7.1101AA	7.1101AB	7.1101AC
----------	----------	----------

IL IL IL IL IL IL IL IL





down counter

Fig. 7.1101

7.12AA	7.12AB	7.12AC
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Exhibit 7.12

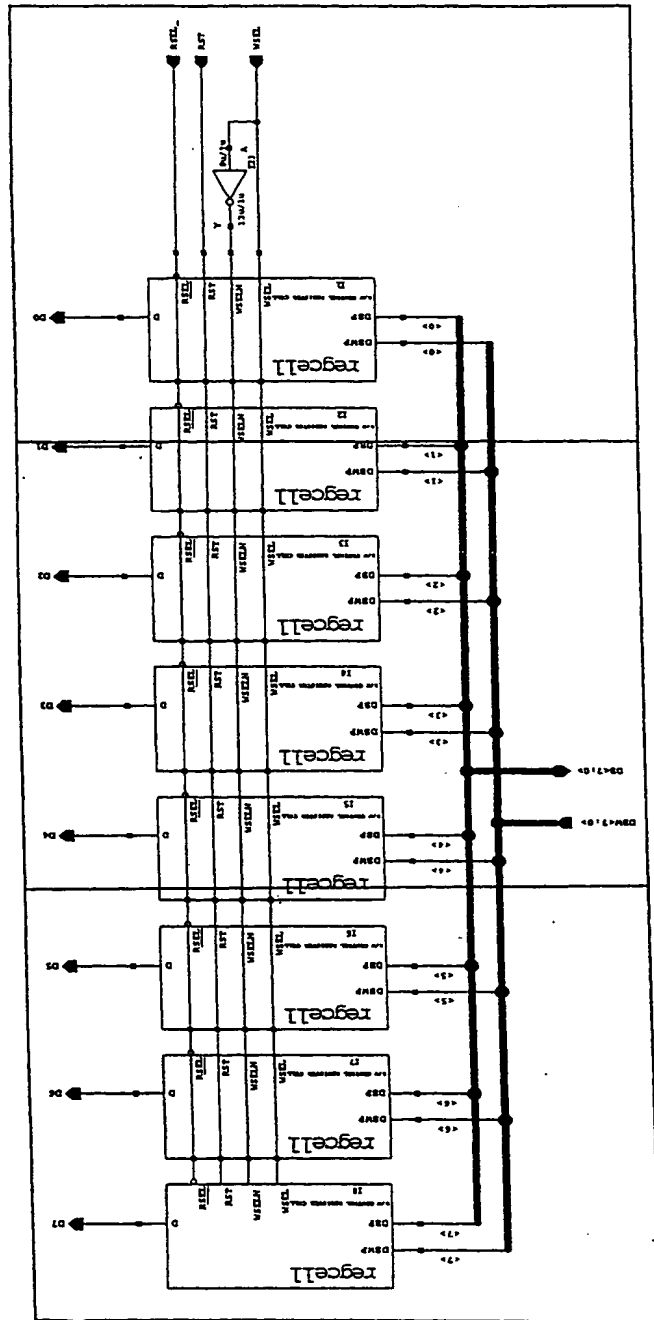
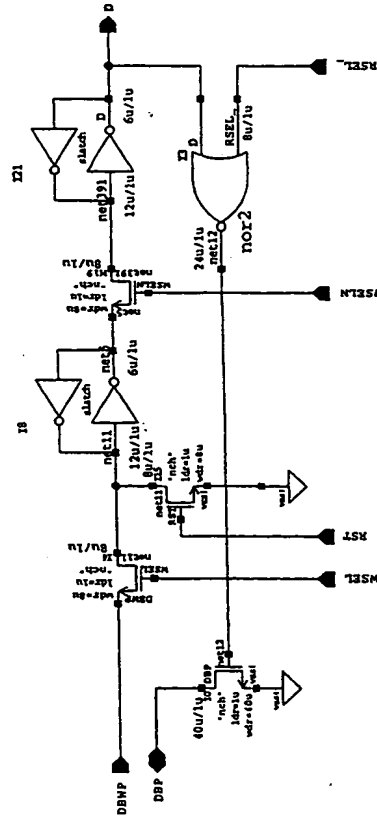


Fig. 7.12

MICRON		PROJECT: L03	DESIGNED: Rotzoll
COMMUNICATIONS, INC.		FILE: R/W Control Register	
INTEGRATED CIRCUIT DESIGN		DATE: 10/14/93	REV: 1
CONFIDENTIAL INFORMATION		DATE: Nov 12 09:44:40 1993	TIME: 11:11

Fig. 7.1201



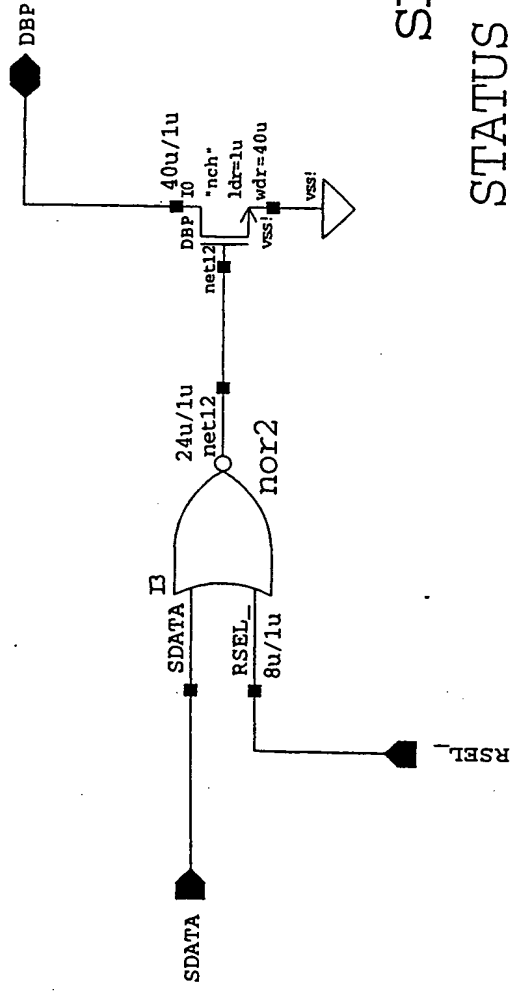
PROJECT: L03		DESIGNER: Rotzoll	
TITLE: R/W Control Register Cell		NAME: 103reva/regcell	
DATE: Nov 12 09:41:36 1993		REV: -	
CONFIDENTIAL INFORMATION		PAGE: A	

7.13AA

7.13BA

END 7.13





sregcell

STATUS REGISTER CELL

R. Rotzoll

12/8/92

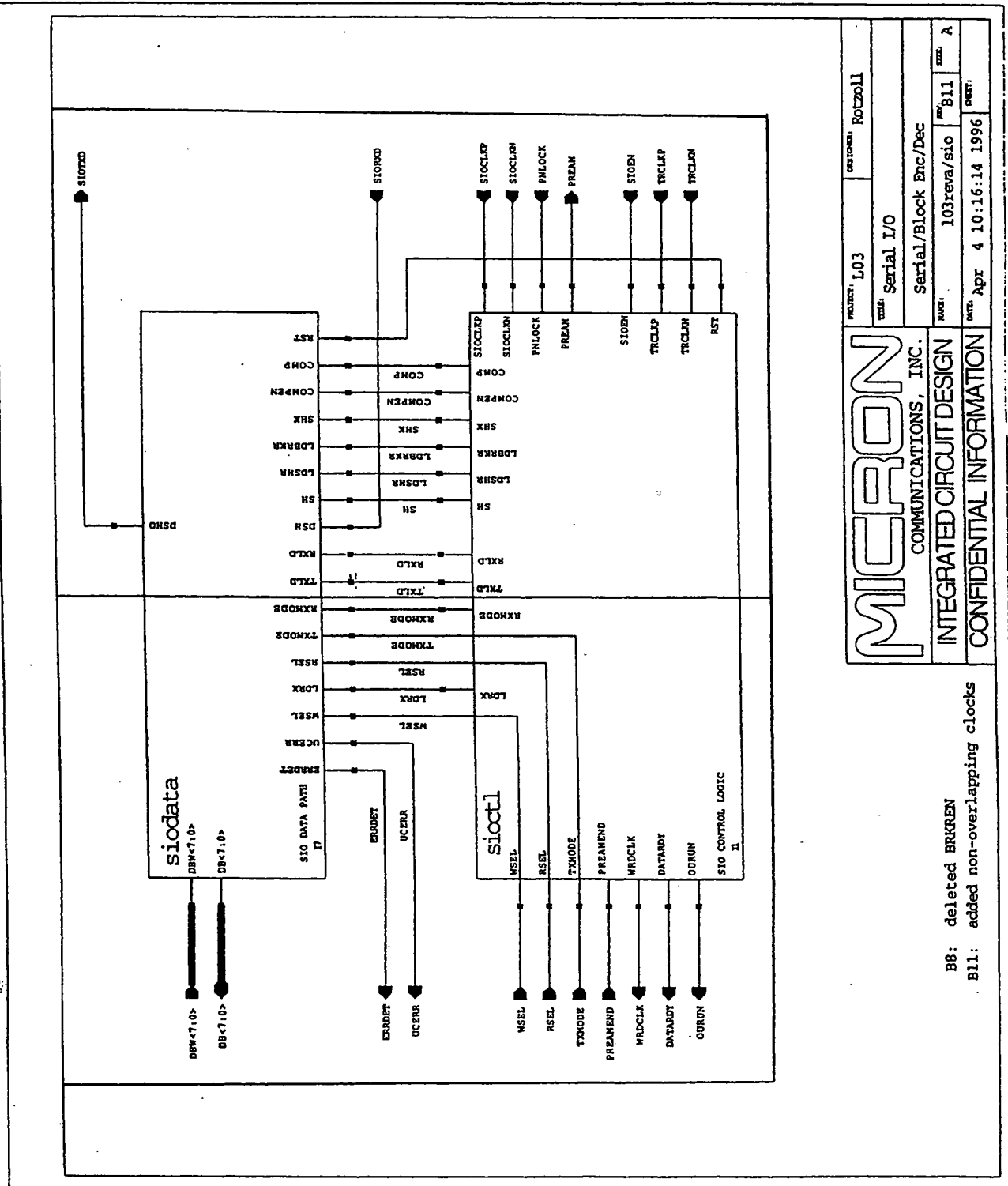
FIG. 7.1301

7.14AB	7.14AA
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Exhibit 7.14



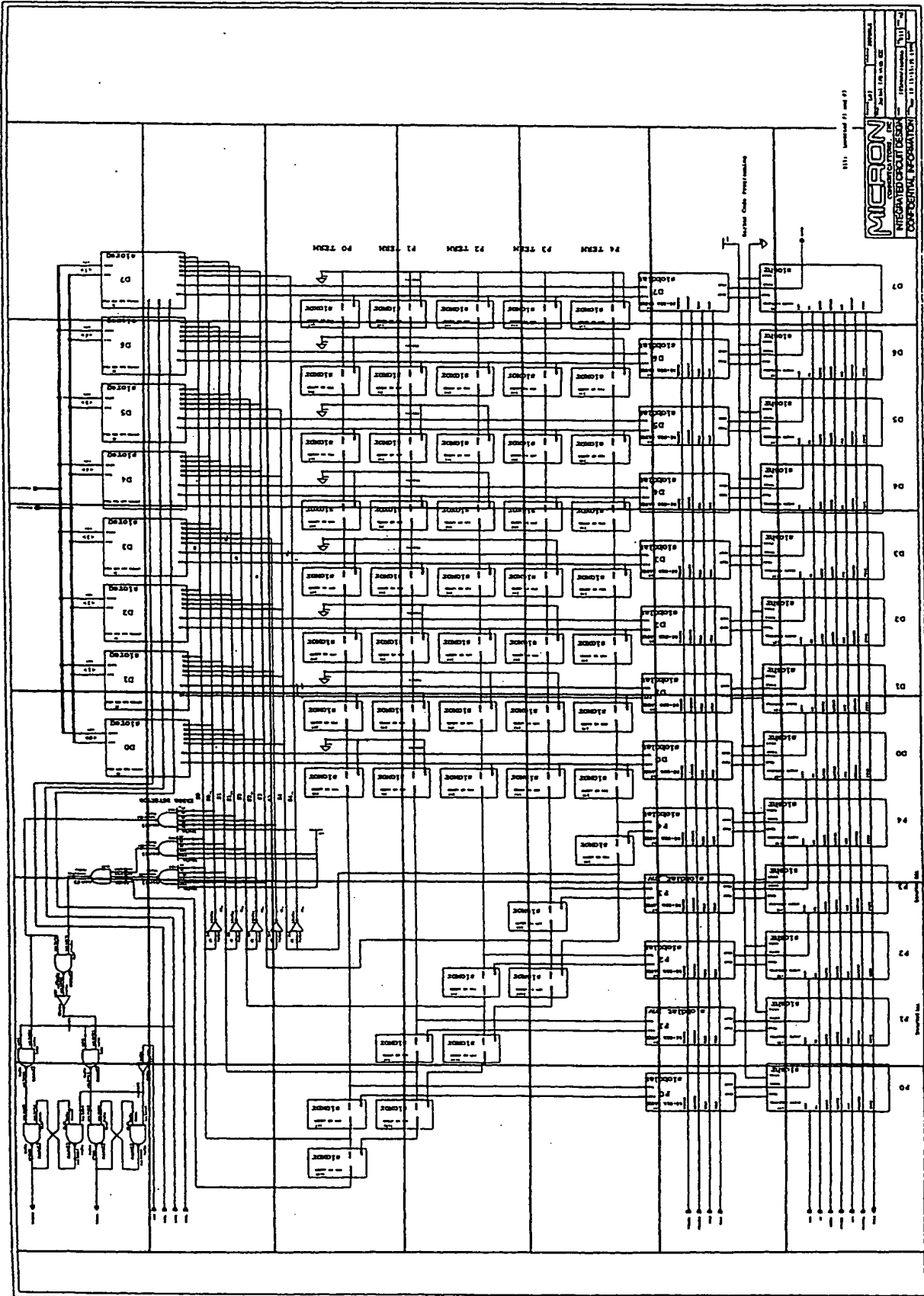
FIG. 7.14



7.1401AA	7.1401AB	7.1401AC	7.1401AD	7.1401AE	7.1401AF
7.1401BA	7.1401BB	7.1401BC	7.1401BD	7.1401BE	7.1401BF
7.1401CA	7.1401CB	7.1401CC	7.1401CD	7.1401CE	7.1401CF
7.1401DA	7.1401DB	7.1401DC	7.1401DD	7.1401DE	7.1401DF
7.1401EA	7.1401EB	7.1401EC	7.1401ED	7.1401EE	7.1401EF
7.1401FA	7.1401FB	7.1401FC	7.1401FD	7.1401FE	7.1401FF
7.1401GA	7.1401GB	7.1401GC	7.1401GD	7.1401GE	7.1401GF

II II II II II II

Fig. 7/1401



100% Functional Test

**MICRON**  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

7.140101AA	7.140101AB
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II II II II II II II

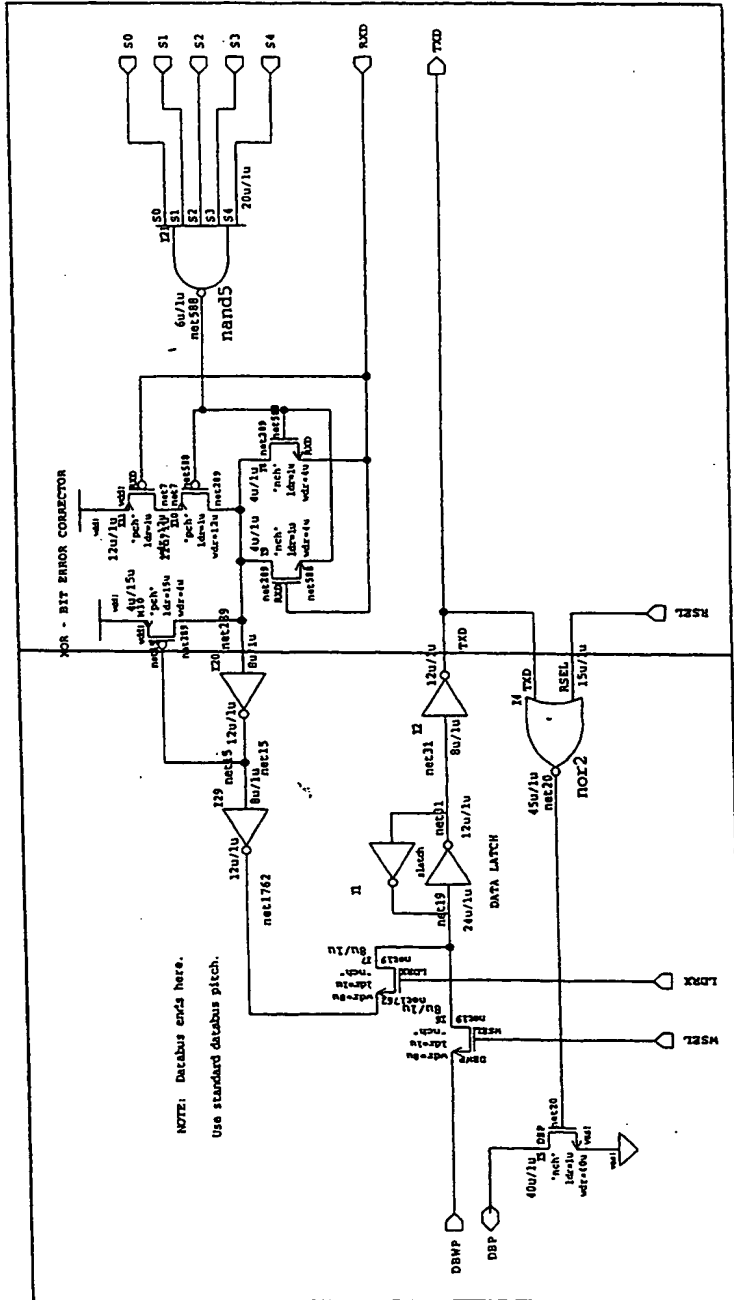


Fig. 7.140101

MICRON		PROJECT: L03		DESIGNER: JOTOOLE	
		TITLE: Serial I/O Register Cell			
		NAME: 103reva/sioreg		REV: B1	
				STN: A	
		DATE: Sep 1 18:03:52 1994		PAGES: 1	

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

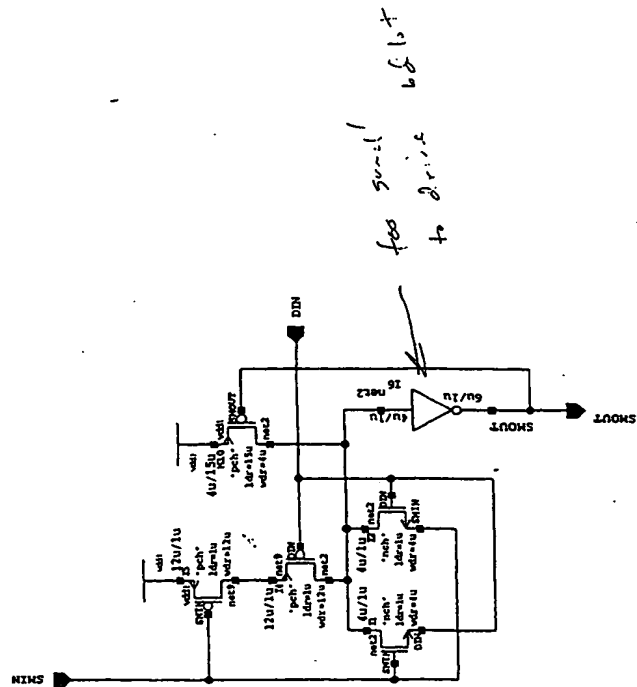


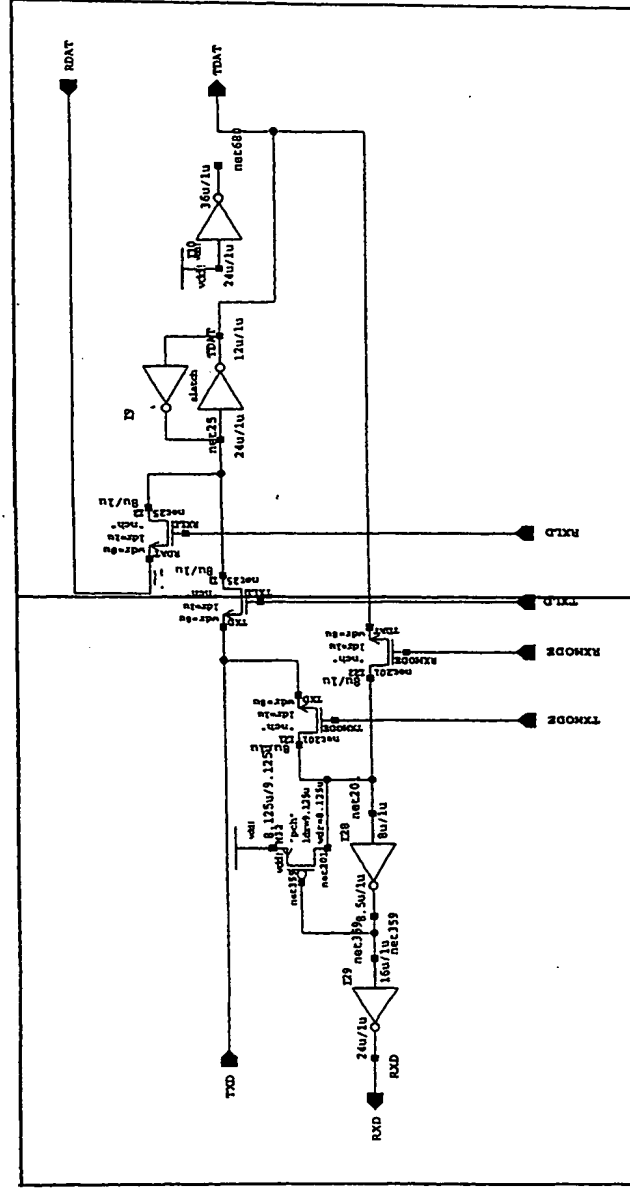
Fig. 7.190102

MICRON		PROJECT: L03	REVISION: JOTOOLE
COMMUNICATIONS, INC.		TITLE: SIO XOR	
INTEGRATED CIRCUIT DESIGN		NAME: 103revA/sioxor	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 1 18:07:22 1994	SHEET: A

7.140103AA	7.140103AB
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II II II II II II II II

Fig. 7.140103



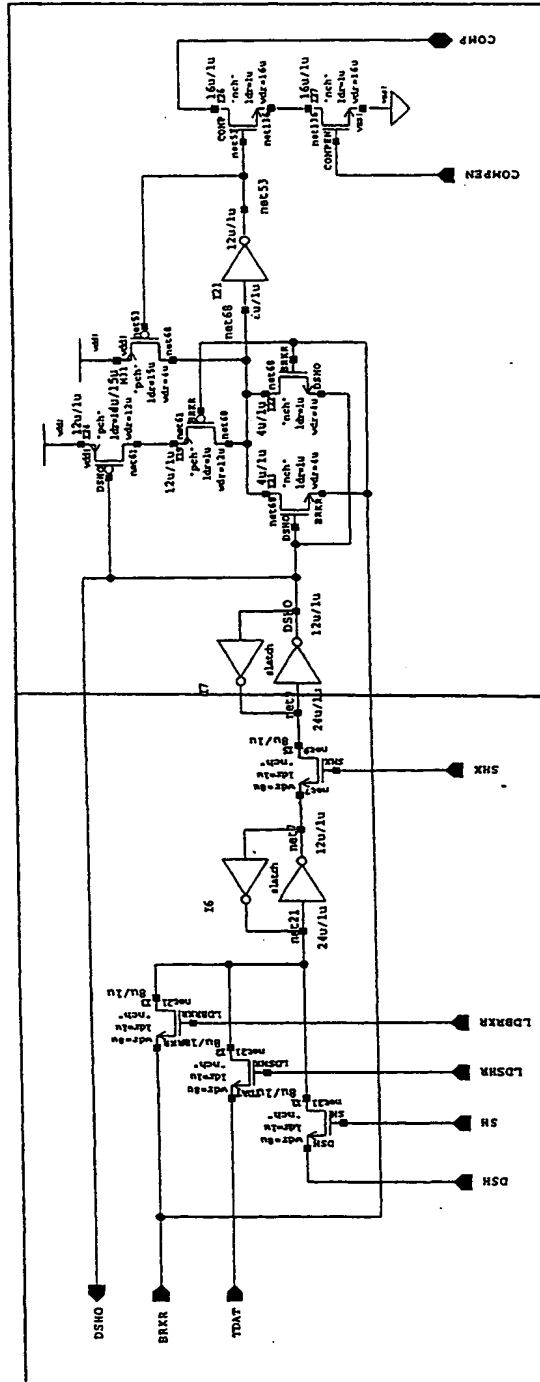
MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: SIO Bidirectional Latch	
INTEGRATED CIRCUIT DESIGN		NAME: _l03revA/siobdlat_inv	REV: B11
CONFIDENTIAL INFORMATION		DATE: Apr 10 15:13:59 1996	BY: A

B11: inverted bit



7.140104AA	7.140104AB
------------	------------

SECRET 7.140104



7.140104

Fig. 7.140104

MICRON		PRODUCT	L03	DESIGNER	JOTOOLE
COMMUNICATIONS, INC.		TITLE	SIO Shift Register		
INTEGRATED CIRCUIT DESIGN		NAME	103reva/sioshr	REV. B1	REV. A
CONFIDENTIAL INFORMATION		DATE	Sep 2 08:06:26 1994		

7.140105AA	7.140105AB
------------	------------

EX-1101105



7.1402AC	7.1402AD	7.1402AE	7.1402AF	7.1402AG	7.1402AH	7.1402AI
7.1402BA	7.1402BB	7.1402BC	7.1402BD	7.1402BE	7.1402BF	7.1402BI
7.1402CA	7.1402CB	7.1402CC	7.1402CD	7.1402CE	7.1402CF	7.1402CI
7.1402DA	7.1402DB	7.1402DC	7.1402DD	7.1402DE	7.1402DF	7.1402DI
7.1402EA	7.1402EB	7.1402EC	7.1402ED	7.1402EE	7.1402EF	7.1402EI

2077.7.11

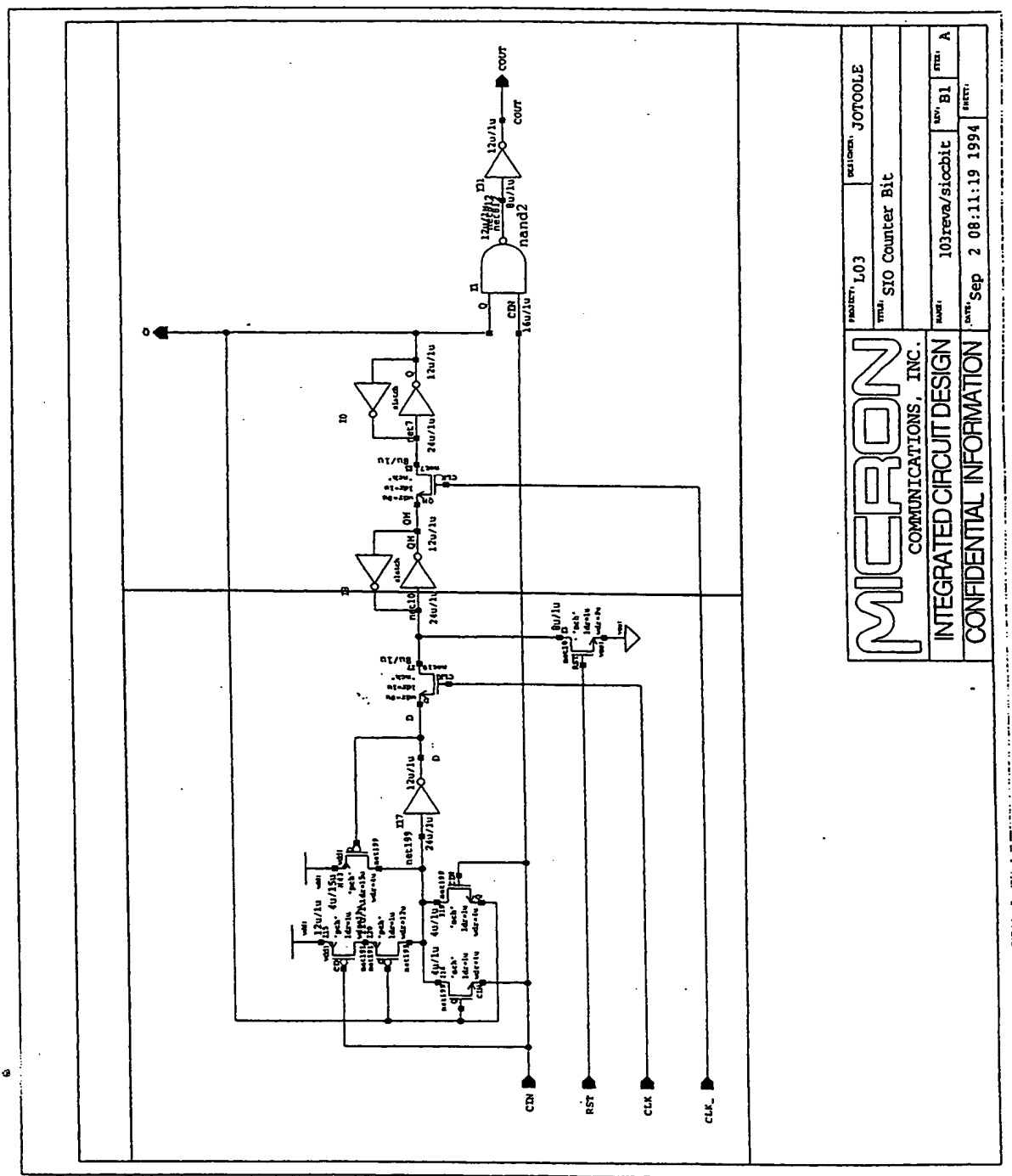


7.140201AA	7.140201AB
------------	------------

## 7.140201AA

[illegible]

201  
Fig. 7.140



<b>MICRON</b>		PROJECT: L03	REVISION: J07000LE
COMMUNICATIONS, INC.		TITLE: SIO Counter Bit	
INTEGRATED CIRCUIT DESIGN		DATE: 103rev/sicbit	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 2 08:11:19 1994	REV: A



7.15AA	7.15AB	7.15AC	7.15AD
7.15BA	7.15BB	7.15BC	7.15BD
7.15CA	7.15CB	7.15CC	7.15CD
7.15DA	7.15DB	7.15DC	7.15DD
7.15EA	7.15EB	7.15EC	

EE 7.15

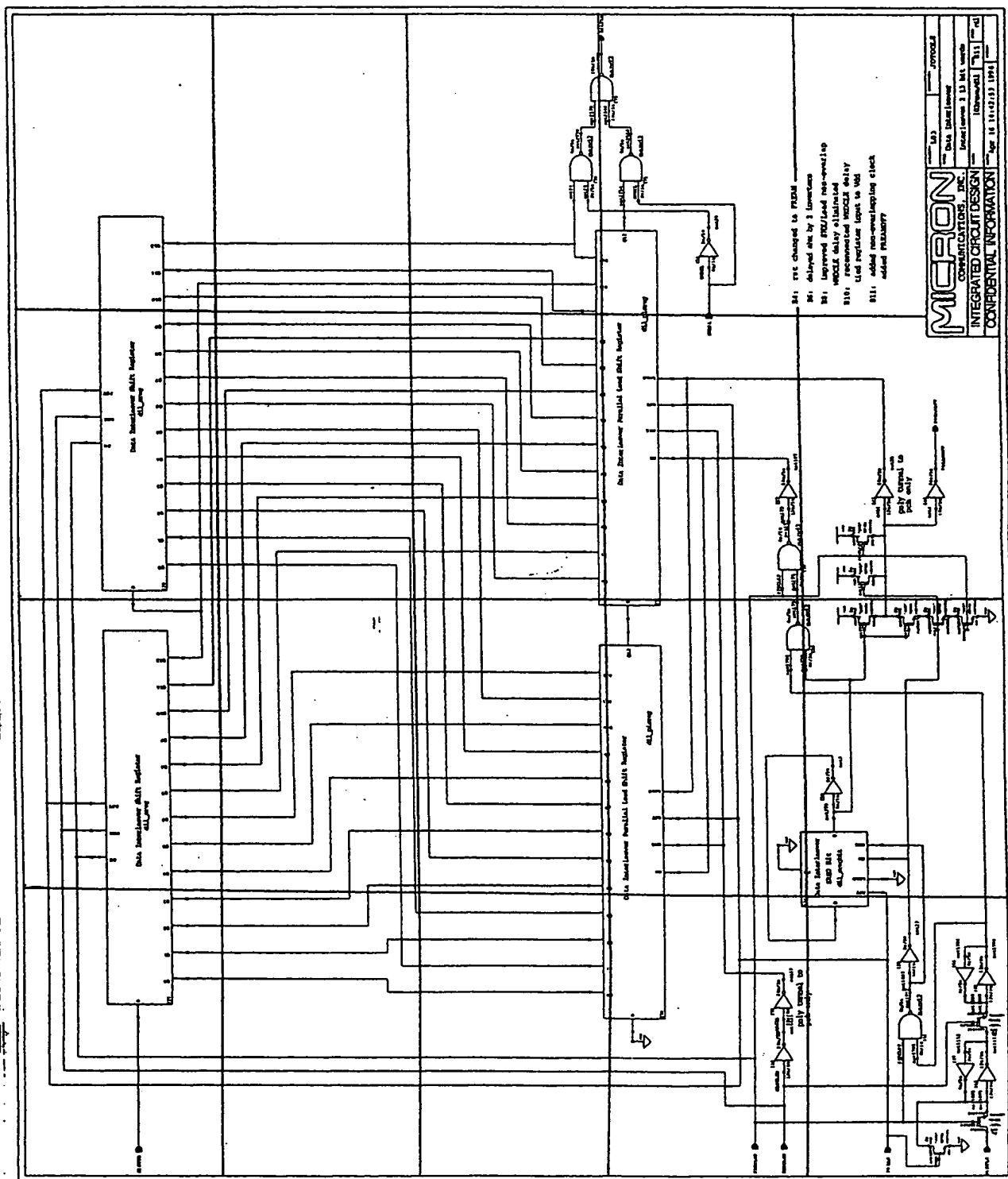


Fig. 7.15

7.1501AA

7.1501BA

7.1501CA

EEG 7.1501

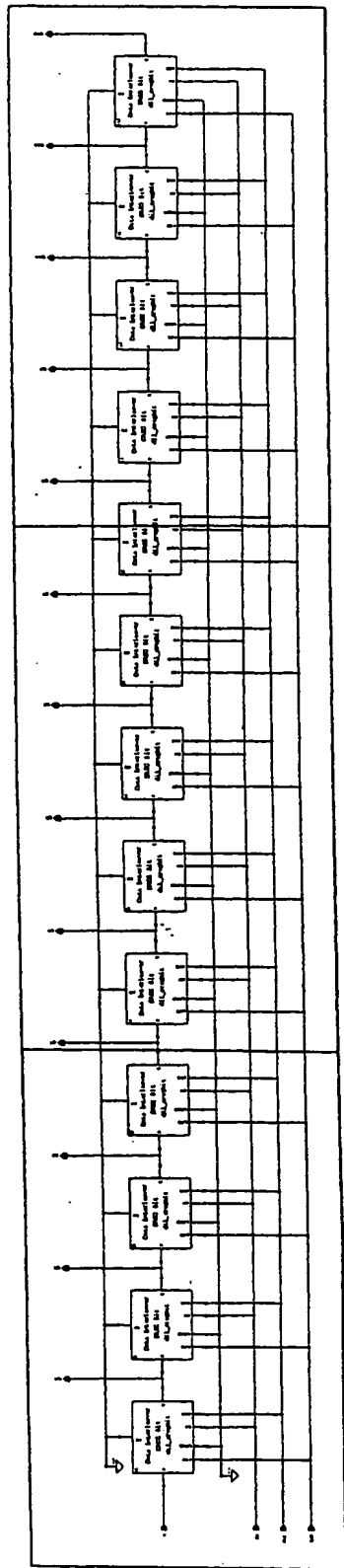


Fig. 7.1501

7.1502AA

7.1502BA

7.1502CA

Fig 7.1502

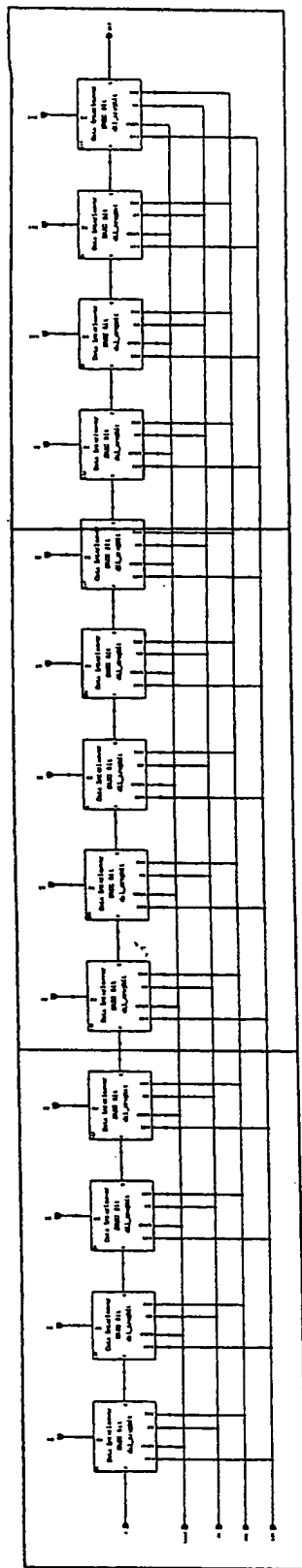
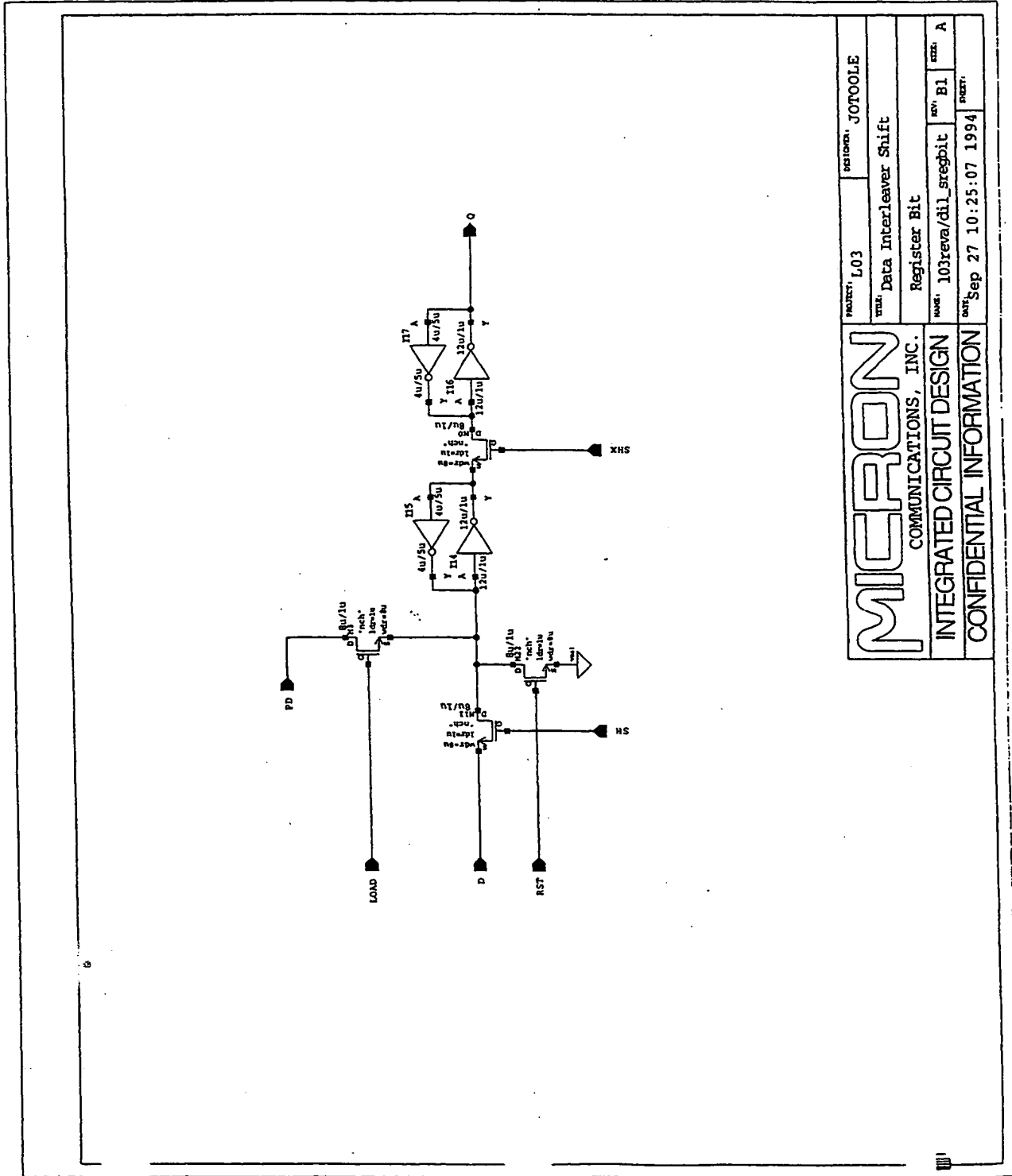


Fig. 7.1502

Fig. 7/50201



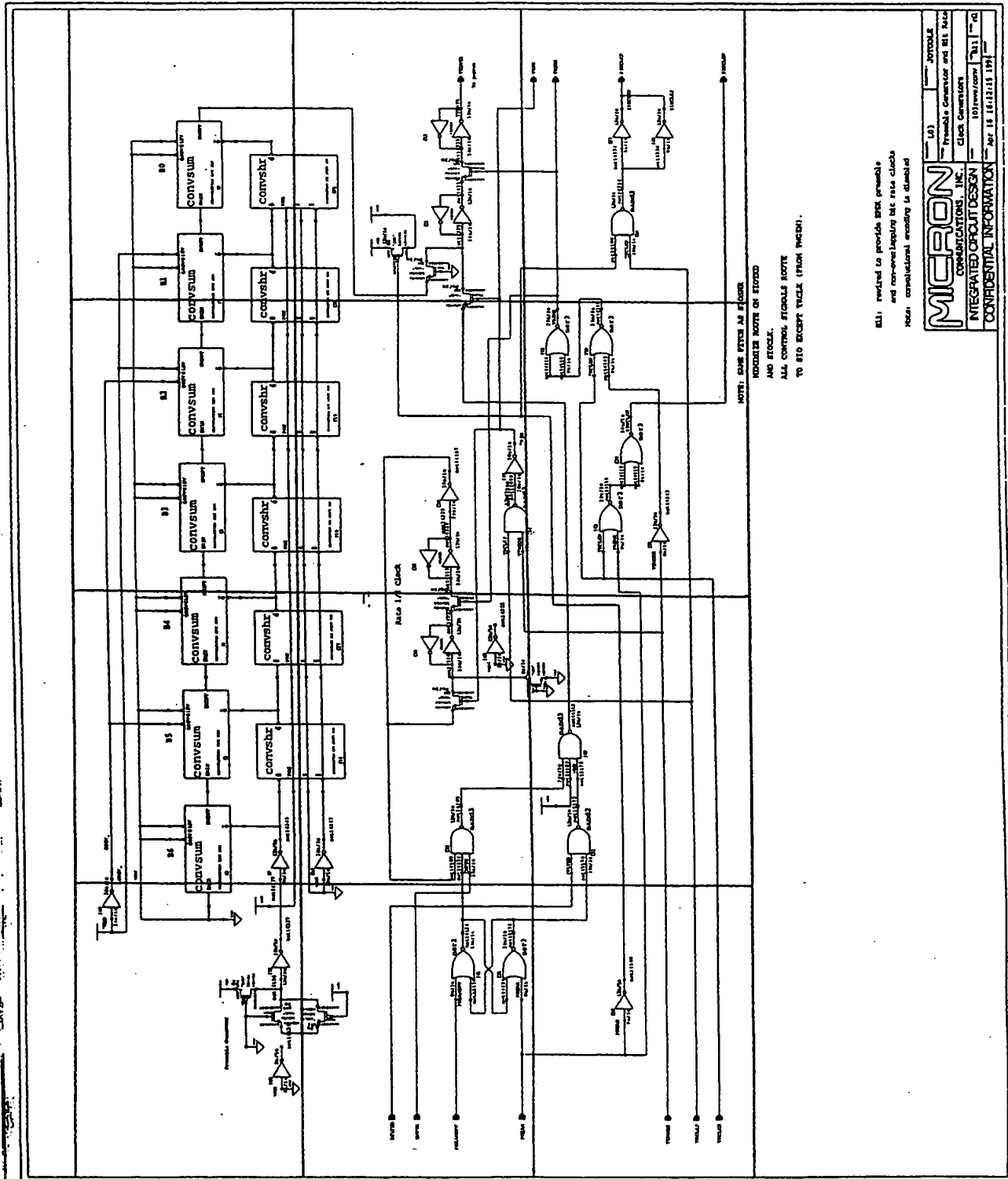
PROJECT: L03		DESIGN: J07001E	
TITLE: Data Interleaver Shift		REV: B1	
REGISTER: Bit		REV: A	
MADE: 103revs/dil_sregbit		REV: B1	
DATE: Sep 27 10:25:07 1994		PAGE: 1	
CONFIDENTIAL INFORMATION			

7.16AA	7.16AB	7.16AC	7.16AD
7.16BA	7.16BB	7.16BC	7.16BD
7.16CA	7.16CB	7.16CC	7.16CD

IL 1015



Fig. 7.16

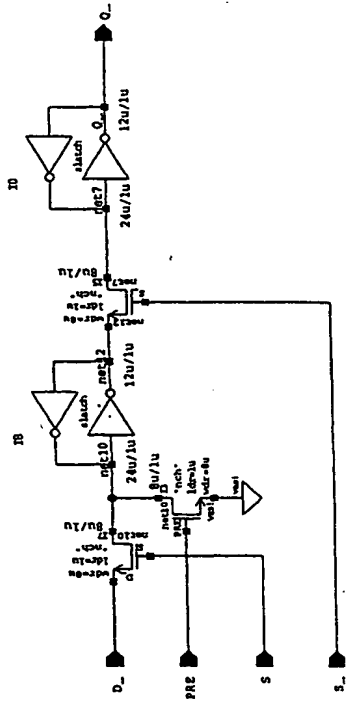


ALL required to provide SPEC. preamble  
and non-overlapping bit rate clock  
Note: convolutional encoding is disabled

<b>MICRON</b>		163	163	163
COMMUNICATIONS, INC.		163	163	163
INTEGRATED CIRCUIT DESIGN		163	163	163
CONFIDENTIAL INFORMATION		163	163	163

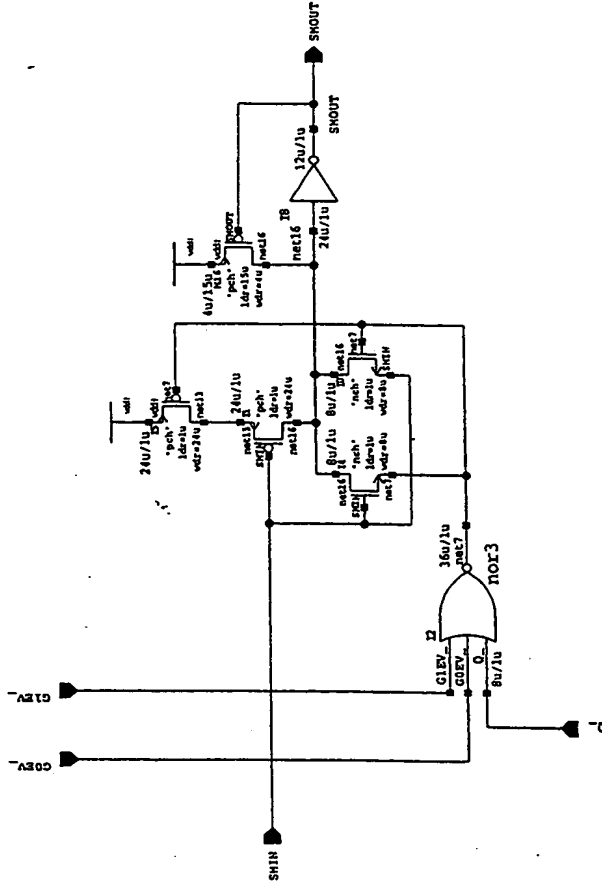
NOTE: DATA FIVE AS FIGURE  
AND CLOCK.  
ALL CONTROL SIGNALS ROUTE  
TO SIO EXCEPT TRAIL (FROM INCH).

Fig. 7.1601



MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: Convolutional Encoder Shift	
INTEGRATED CIRCUIT DESIGN		Register Cell	
CONFIDENTIAL INFORMATION		DATE: 103revA/convshr	REV: A
		DATE: Sep 2 10:34:27 1994	SHEET: 1

Fig. 7.1602



PROJECT: L03		DESIGNER: JOTOOLE	
TITLE: Convolutional Encoder Summer			
MAKER: 103reva/convsum		REV: B1	SIZE: A
DATE: Sep 2 10:32:17 1994		PROJECT:	

**MICRON**  
COMMUNICATIONS, INC.

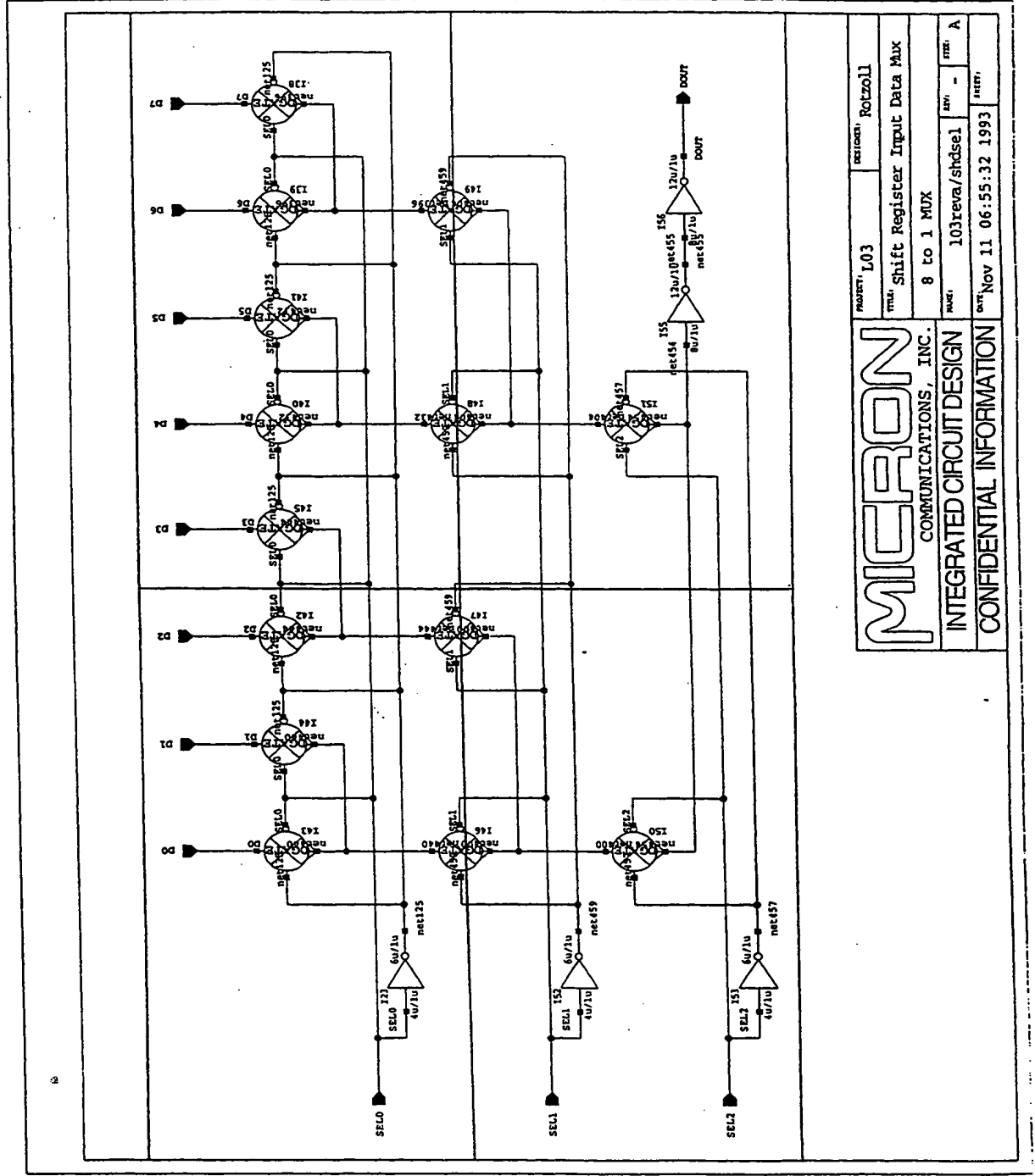
INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

7.17AB	7.17BB
7.17AA	7.17BA

Ex 11.11

Fig. 7.17



MICRON		PROJECT: L03		DESIGNER: Rotzoll	
COMMUNICATIONS, INC.					
INTEGRATED CIRCUIT DESIGN					
CONFIDENTIAL INFORMATION					
NAME:		103revA/shdse1		REV:	-
DATE:		Nov 11 06:55:32 1993		PAGE: 1	

7.18AA	7.18AB	7.18AC
7.18BA	7.18BB	7.18BC
7.18CA	7.18CB	7.18CC

EX-118B

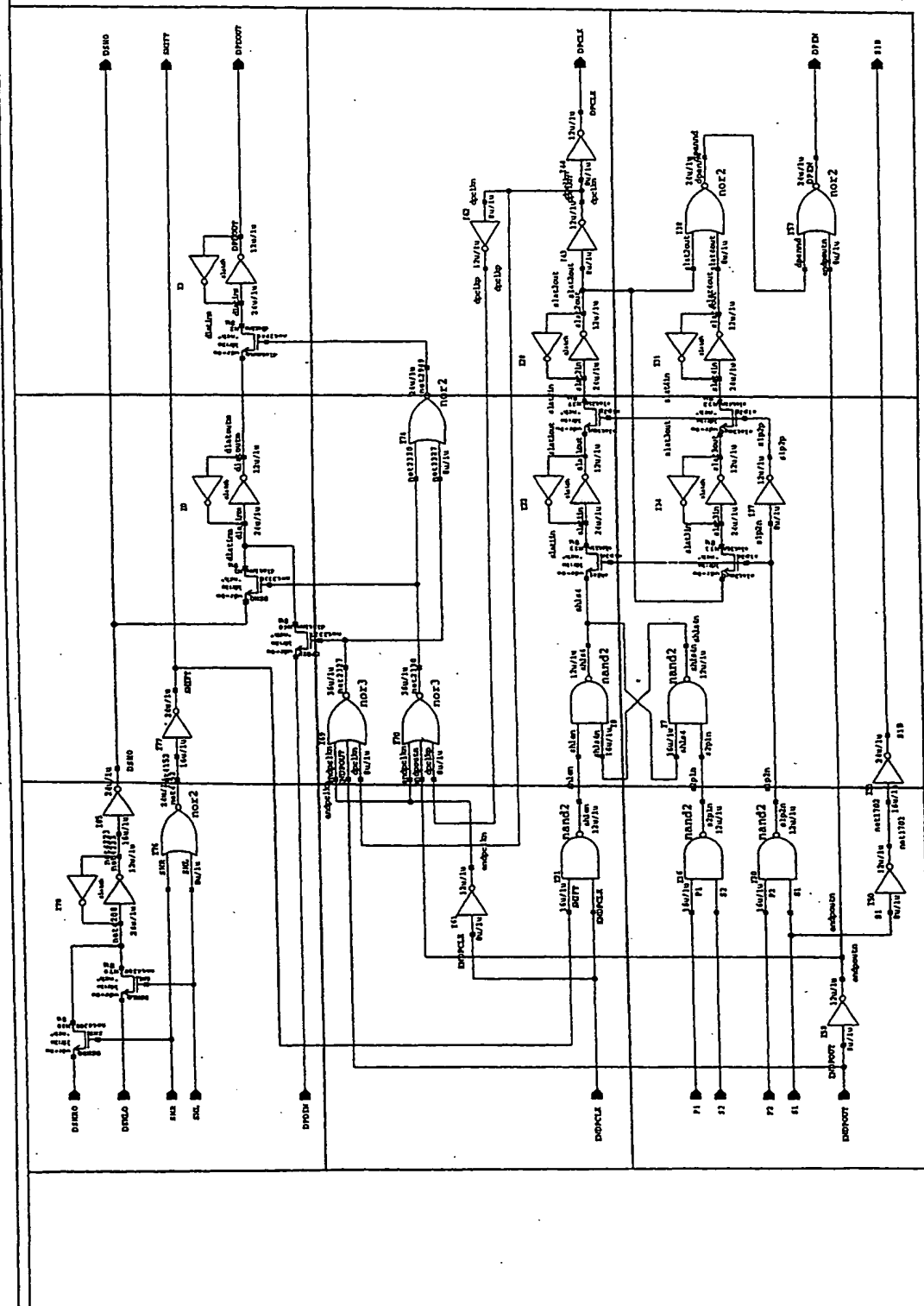


Fig. 7.18

# 2013

**COMMUNICATIONS, INC.**  
**INTEGRATED CIRCUIT DESIGN**

## INTEGRATED CIRCUIT DESIGN

**CONFIDENTIAL INFORMATION**

Page 103

**THE DIGITAL**

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103

Nov 12

8AA	8AB
8BA	8BB
8CA	8CB

IL II BB





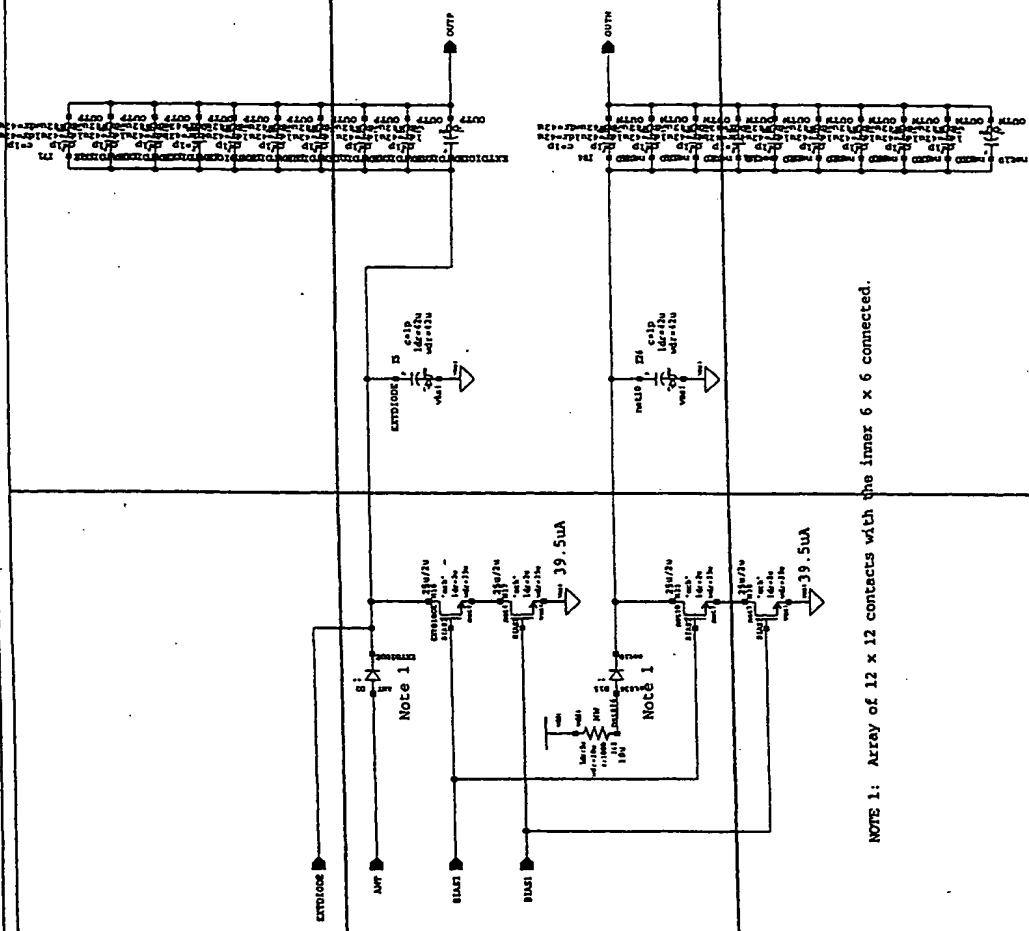
8.01AA	8.01AB	8.01AC	8.01AD	8.01AE
8.01BA	8.01BB	8.01BC	8.01BD	8.01BE
8.01CA	8.01CB	8.01CC	8.01CD	8.01CE
8.01DA	8.01DB	8.01DC	8.01DD	8.01DE

II II II II II II



8.0101AA	8.0101AB
8.0101BA	8.0101BB
8.0101CA	8.0101CB

II II II II II II



NOTE 1: Array of 12 x 12 contacts with the inner 6 x 6 connected.

Fig. 8.0101AA-C8

MICRON		PROPERTY L03	DATE 10/10/10	JOT000LE
COMMUNICATIONS, INC.		Schottky Diode Detector		
INTEGRATED CIRCUIT DESIGN		IBIAS=75uA		
CONFIDENTIAL INFORMATION		B13		
		May 24 13:54:28 1996		

- B2: Connected EXTIOIDE line
- B6: schottky array changed to 6x6  
rf cap reduced to 1pF
- B8: increased Cc to 10pF; decreased Crf to 1pF
- B13: added 1K resistor in series with dummy diode for ESD



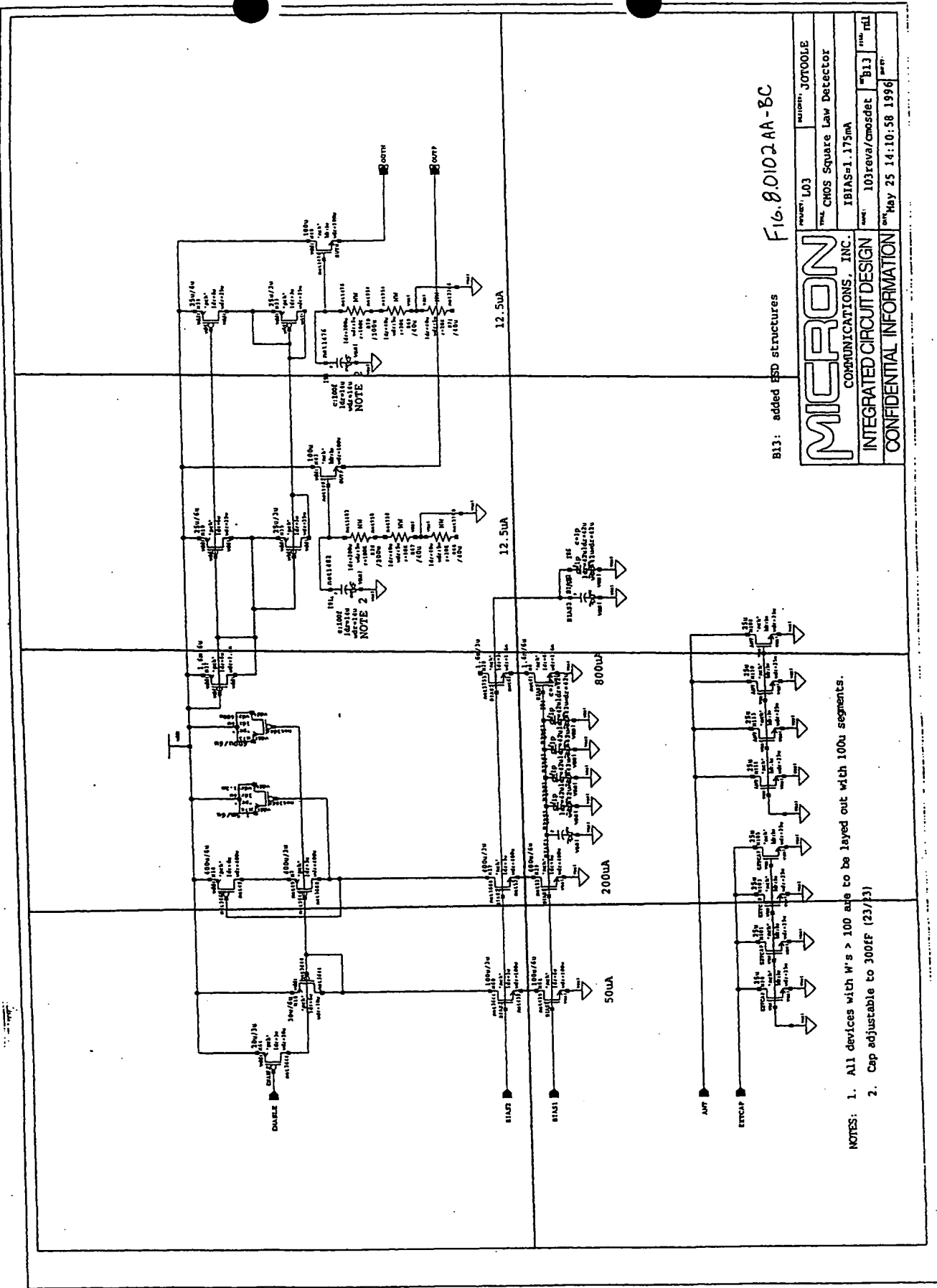


Fig. 8.0102 AA-8C

B13: added BBD structures

MICRON		PROPERTY: L03	DATE: J0700LE
COMMUNICATIONS, INC.		TYPE: CMOS Square Law Detector	
INTEGRATED CIRCUIT DESIGN		IBIAS=1.175mA	
CONFIDENTIAL INFORMATION		DATE: 103rev/cmosdet	"B13" FILE
		DATE: May 25 14:10:58 1996	REV:

- NOTES:
1. All devices with W's > 100 are to be laid out with 100u segments.
  2. Cap adjustable to 300fF (23/33)

8.0103AA	8.0103AB	8.0103AC	8.0103AD	8.0103AE	8.0103AF
8.0103BA	8.0103BB	8.0103BC	8.0103BD	8.0103BE	8.0103BF
8.0103CA	8.0103CB	8.0103CC	8.0103CD	8.0103CE	8.0103CF

SECRET



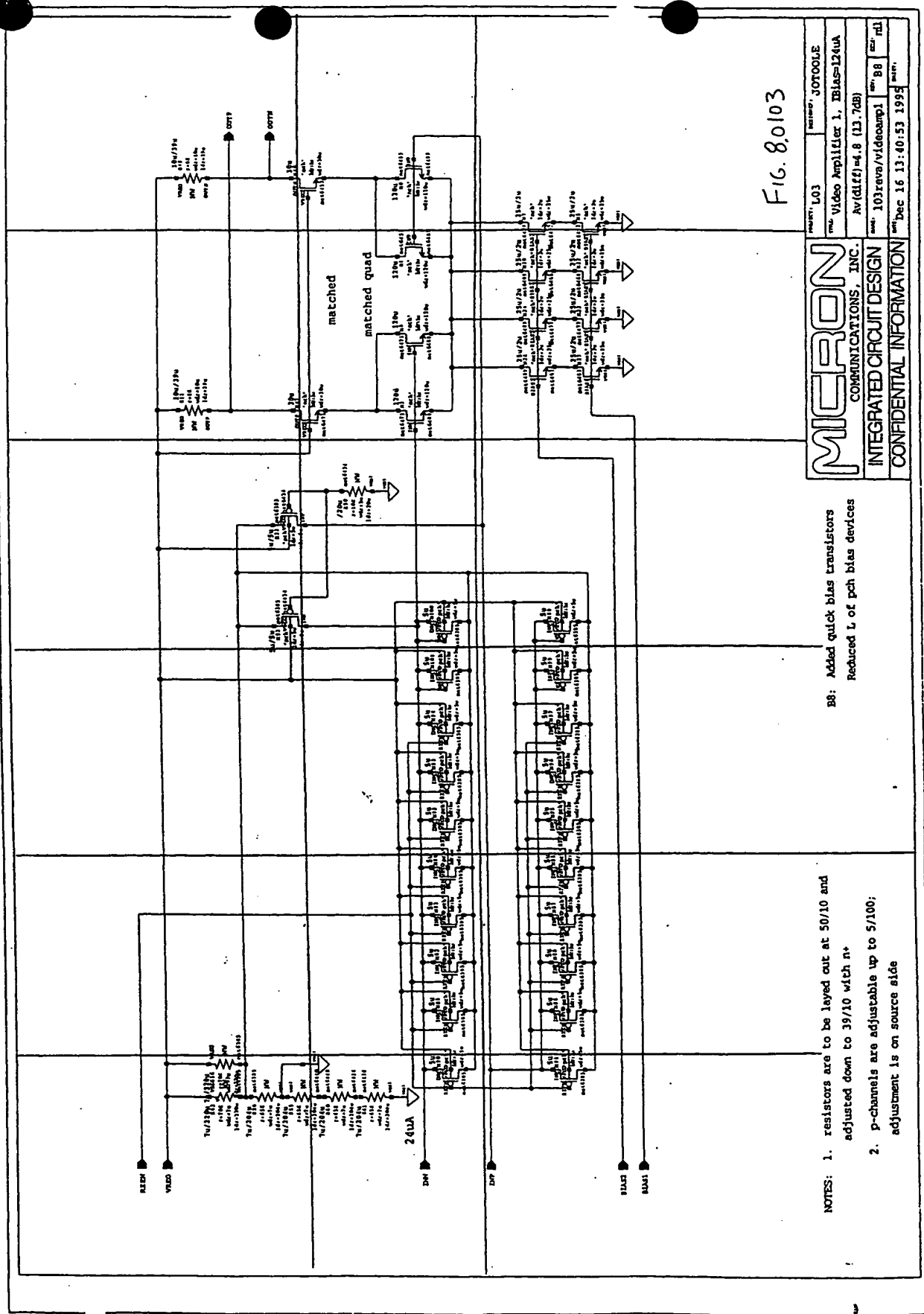


FIG. 8.0103

MICRON	
COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
PROJECT: L03	REVISION: J07000LE
Title: Video Amplifier 1, Bias=124uA	
Av(diff)=4.8 (13.7dB)	
DATE: 10/3/84	DESIGNER: B8
DEC 16 13:40:53 1995	

BB: Added quick bias transistors  
Reduced  $I_{DQ}$  of pch bias devices

- NOTES:
1. resistors are to be layed out at 50/10 and adjusted down to 39/10 with n+
  2. p-channels are adjustable up to 5/100; adjustment is on source side

8.0104AA	8.0104AB	8.0104AC
8.0104BA	8.0104BB	8.0104BC

II II III III III III III III

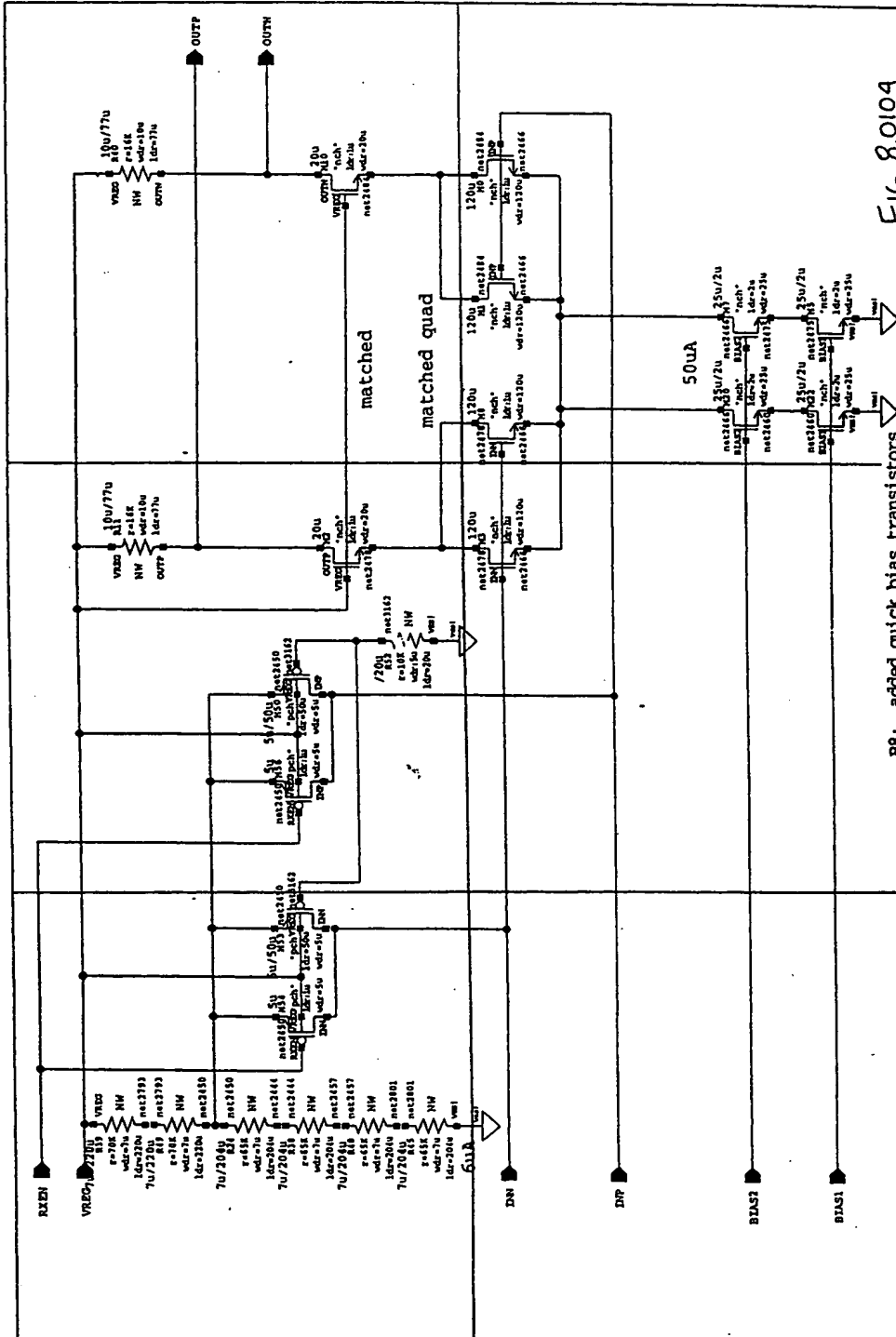


FIG 8.0104

B8: added quick bias transistors

- NOTES:
1. resistors are to be layed out at 100/10 and adjusted down to 77/10 with n+
  2. p-channels are adjustable up to 5/100; adjustment is on the source side.

MICRON	
COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
PROJECT: L03	DESIGNER: JOTOOLE
TITLE: Video Amplifier 2, IBias=56uA	
Av(diff)=5.6 (15dB)	
MODE: 103reva/videoamp2	REV: B8
DATE: Dec 16 13:42:25 1995	
PAGE: 1	

8.0105AA	8.0105AB	8.0105AC	8.0105AD	
8.0105BA	8.0105BB	8.0105BC	8.0105BD	
8.0105CA	8.0105CB	8.0105CC	8.0105CD	8.0105CE
8.0105DA	8.0105DB	8.0105DC	8.0105DD	8.0105DE
8.0105EA	8.0105EB	8.0105EC	8.0105ED	

EE BB DD EE

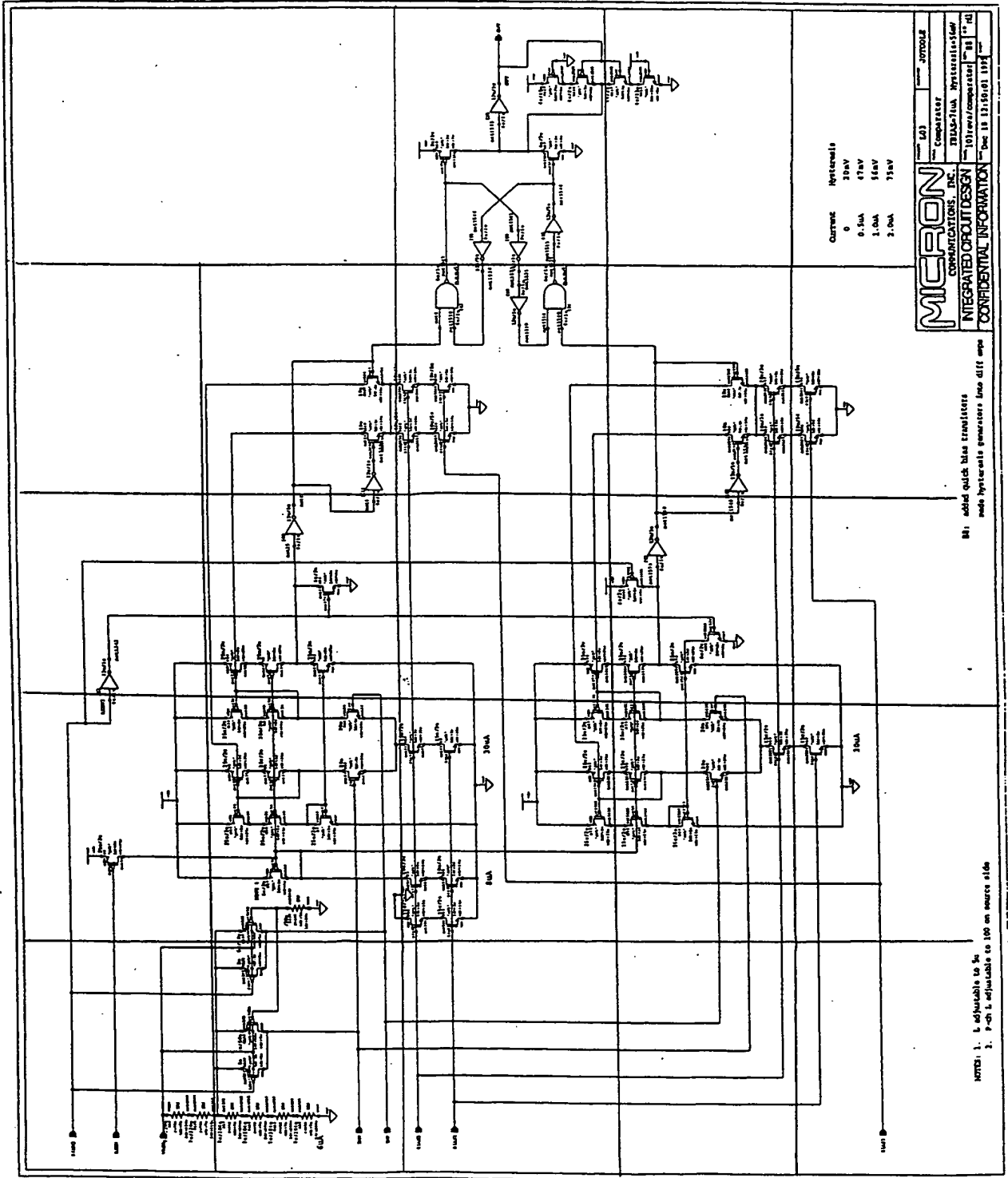


Fig. 8.0105

MICRON	
28L011A	Hysteretolizer
COMPARATORS	INC.
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
Doc 18 1115061 1971	

M1: added quick bias transistors  
 made hysteretolizer generators into diff amp

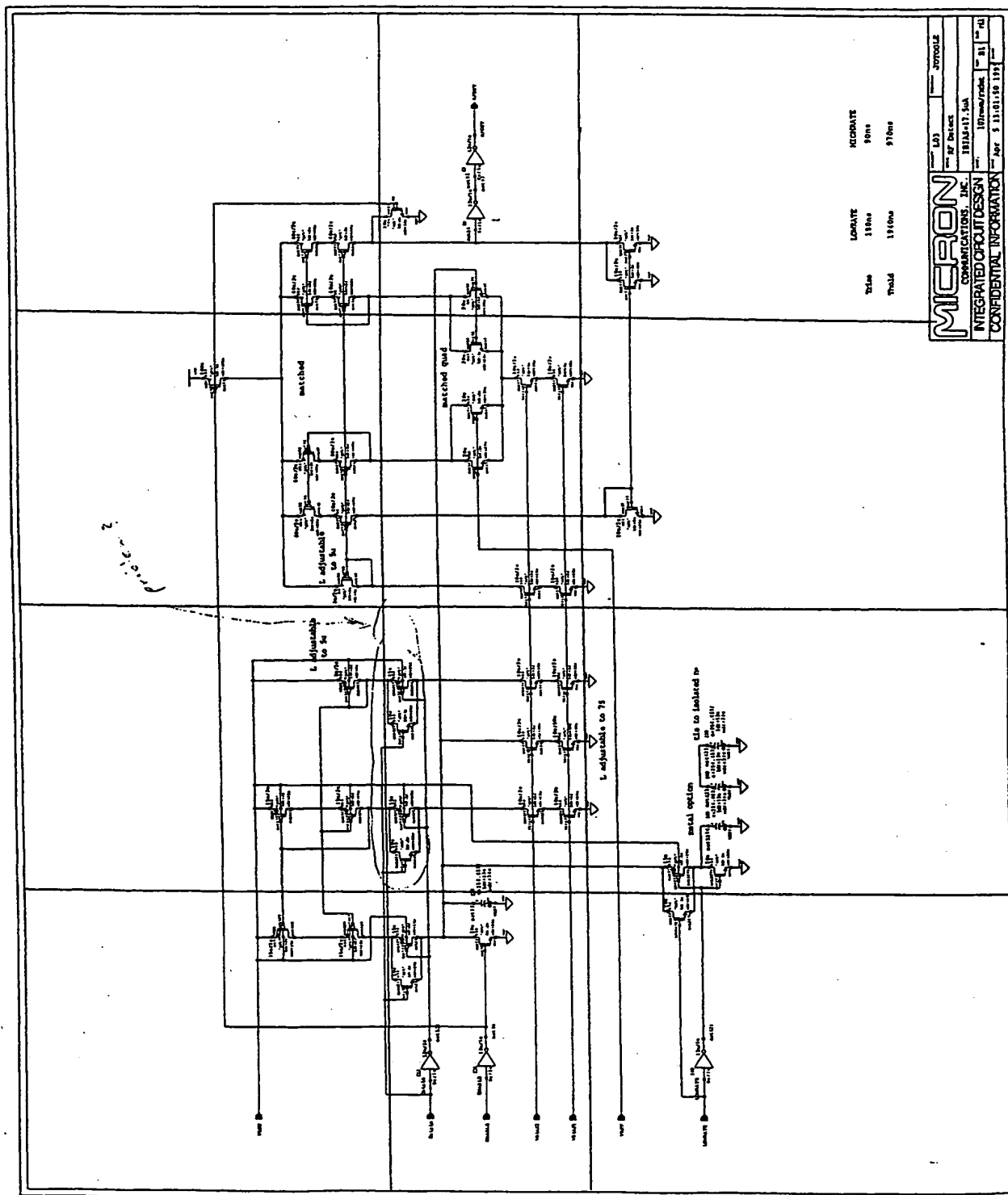
NOTES: 1. L adjustable to 5k  
 2. P-dn L adjustable to 100 on source side

Current	Hysteretol
0	30uV
0.5uA	47uV
1.0uA	56uV
2.0uA	73uV

8.0106AA	8.0106AB	8.0106AC	8.0106AD
8.0106BA	8.0106BB	8.0106BC	8.0106BD
8.0106CA	8.0106CB	8.0106CC	8.0106CD

EE BB.0106

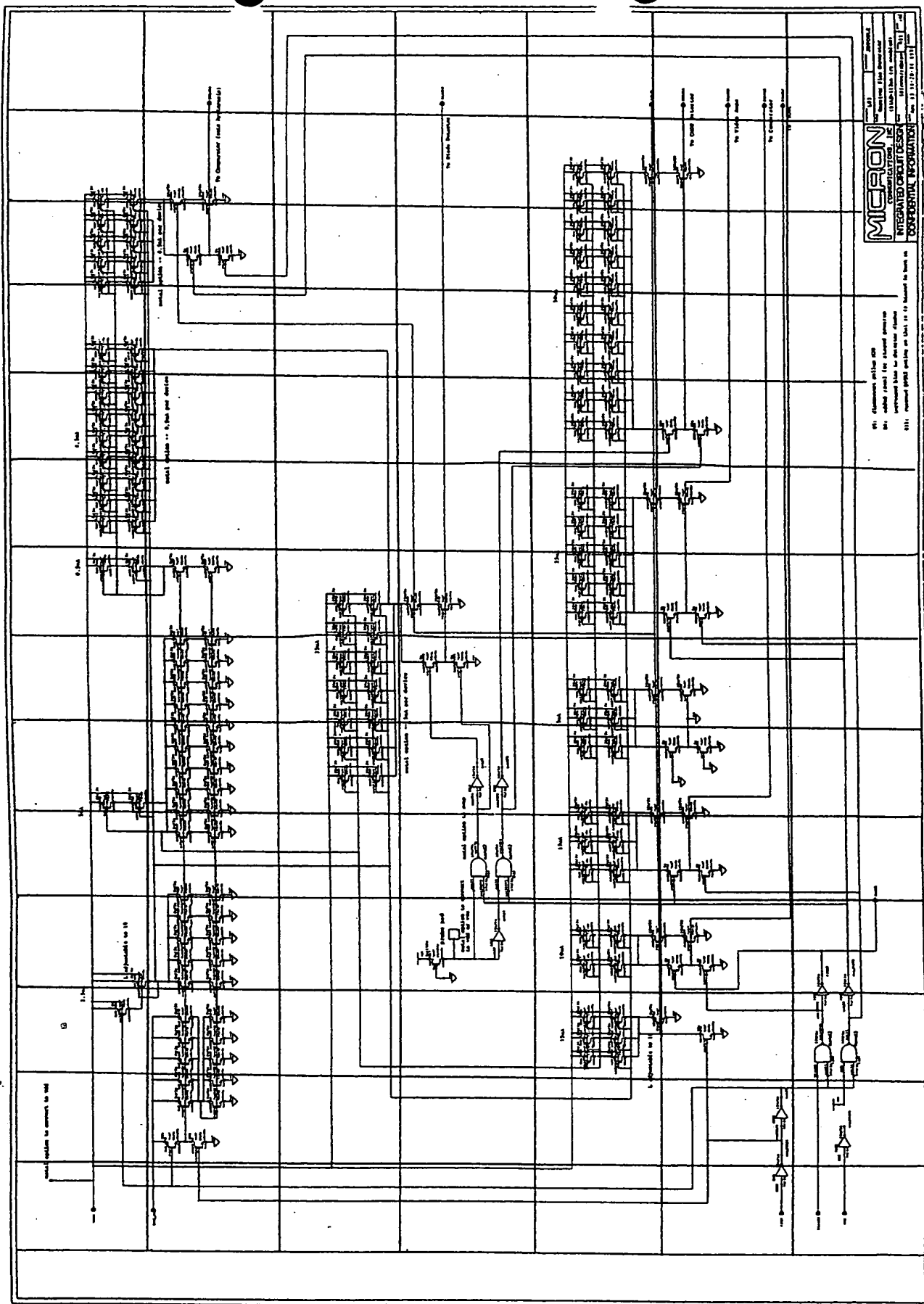
FIG. 8.0106



8.0107AA	8.0107AB	8.0107AC	8.0107AD	8.0107AE	8.0107AF	8.0107AG	8.0107AH	8.0107AI	8.0107AJ	8.0107AK	8.0107AL	8.0107AM
8.0107BA	8.0107BB	8.0107BC	8.0107BD	8.0107BE	8.0107BF	8.0107BG	8.0107BH	8.0107BI	8.0107BJ	8.0107BK	8.0107BL	8.0107BM
8.0107CA	8.0107CB	8.0107CC	8.0107CD	8.0107CE	8.0107CF	8.0107CG	8.0107CH	8.0107CI	8.0107CJ	8.0107CK	8.0107CL	8.0107CM
8.0107DA	8.0107DB	8.0107DC	8.0107DD	8.0107DE	8.0107DF	8.0107DG	8.0107DH	8.0107DI	8.0107DJ	8.0107DK	8.0107DL	8.0107DM
8.0107EA	8.0107EB	8.0107EC	8.0107ED	8.0107EE	8.0107EF	8.0107EG	8.0107EH	8.0107EI	8.0107EJ	8.0107EK	8.0107EL	8.0107EM
8.0107FA	8.0107FB	8.0107FC	8.0107FD	8.0107FE	8.0107FF	8.0107FG	8.0107FH	8.0107FI	8.0107FJ	8.0107FK	8.0107FL	8.0107FM
8.0107GA	8.0107GB	8.0107GC	8.0107GD	8.0107GE	8.0107GF	8.0107GG	8.0107GH	8.0107GI	8.0107GJ	8.0107GK	8.0107GL	8.0107GM
												8.0107GN


 DEPT. OF DEFENSE





**MURON**  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION  
 DATE: 12-17-73  
 BY: [illegible]  
 CHECKED: [illegible]  
 APPROVED: [illegible]

Fig. 16. K. 0107

8.0108AC	8.0108AB	8.0108AA
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8.0108

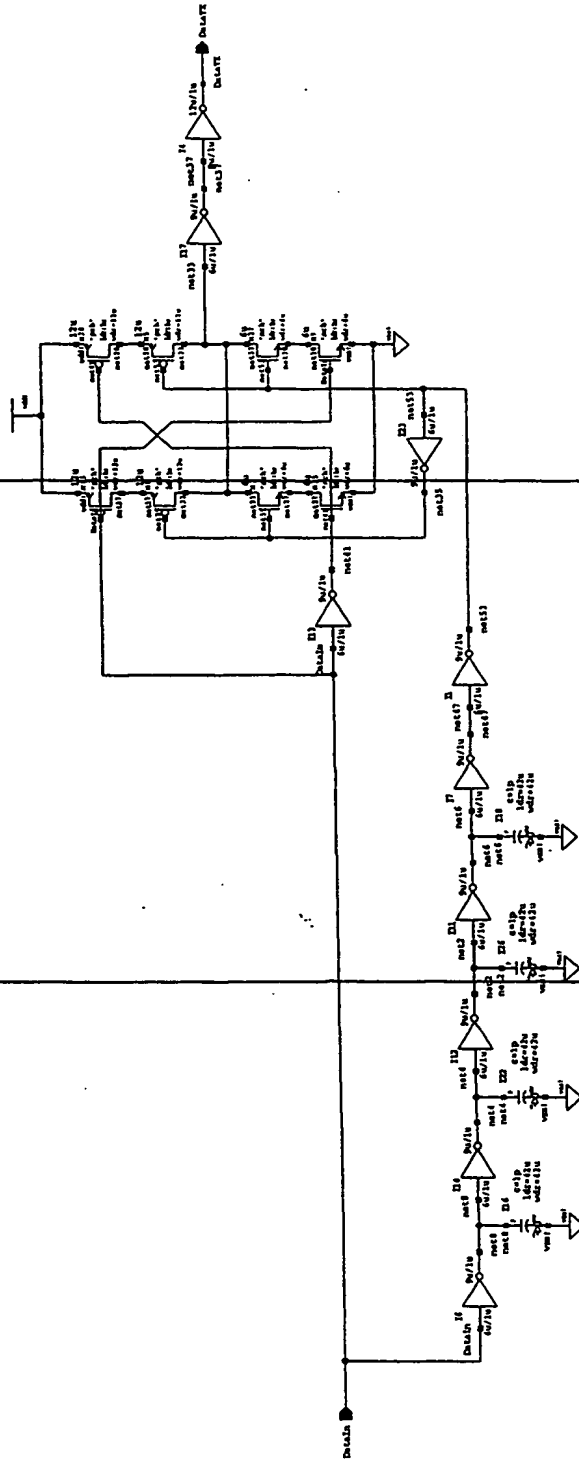


FIG. 8.0108.

# 2001

**COMMUNICATIONS, INC.**

**INTEGRATED CIRCUIT DESIGN**

**CONFIDENTIAL INFORMATION**

NAME JOTOLE

TIME	Data Transition Detector
0000	0000
0001	0001
0002	0002
0003	0003
0004	0004
0005	0005
0006	0006
0007	0007
0008	0008
0009	0009
0010	0010
0011	0011
0012	0012
0013	0013
0014	0014
0015	0015
0016	0016
0017	0017
0018	0018
0019	0019
0020	0020
0021	0021
0022	0022
0023	0023
0024	0024
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0043	0043
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0067	0067
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0069	0069
0070	0070
0071	0071
0072	0072
0073	0073
0074	0074
0075	0075
0076	0076
0077	0077
0078	0078
0079	0079
0080	0080
0081	0081
0082	0082
0083	0083
0084	0084
0085	0085
0086	0086
0087	0087
0088	0088
0089	0089
0090	0090
0091	0091
0092	0092
0093	0093
0094	0094
0095	0095
0096	0096
0097	0097
0098	0098
0099	0099

Output Pulse Width = 40ns (nom)

name:	103reva/databx	rev. B1	72 ml
-------	----------------	---------	-------

11/16, Dec 14 17:11:15 1994

[illegible]

8.02AA	8.02AB	8.02AC
8.02BA	8.02BB	8.02BC

EX-88

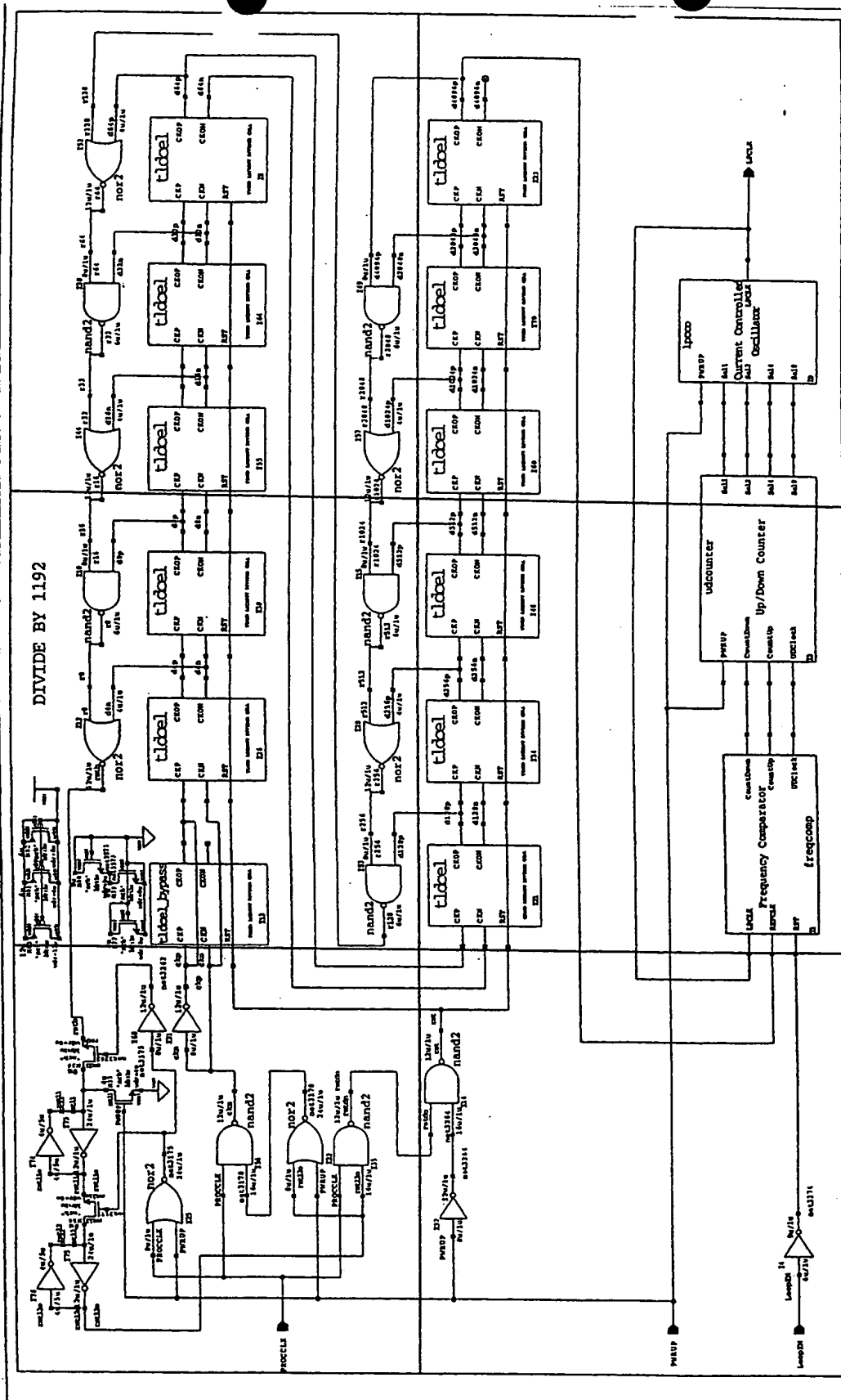


Fig. 8.02

MICRON		PROPERTY 103	REVISED J0700LE
COMMUNICATIONS, INC.		Low Power PLL (1ab-55na typ)	
INTEGRATED CIRCUIT DESIGN		Line 9: 5375kHz / fout=8000Hz	
CONFIDENTIAL INFORMATION		100rev/021	7310
		Mar 26 16:14:18 1996	

B10: first divider stage bypassed

8.0201AB

8.0201AA

II II III III III III III III



8.0202AA	8.0202AB	8.0202AC	8.0202AD
8.0202BA	8.0202BB	8.0202BC	8.0202BD
8.0202CA	8.0202CB	8.0202CC	8.0202CD

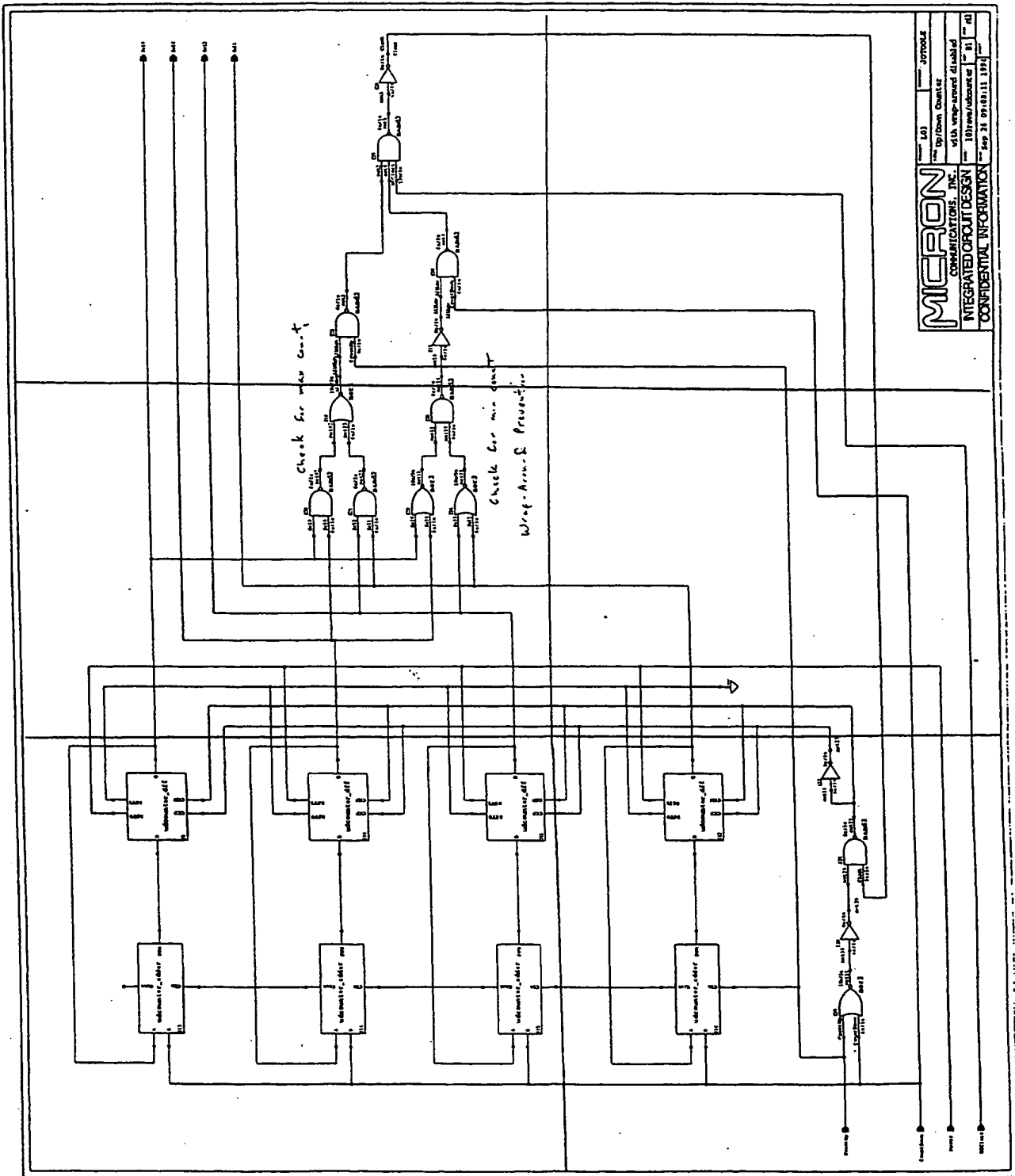
II II II II II II II II





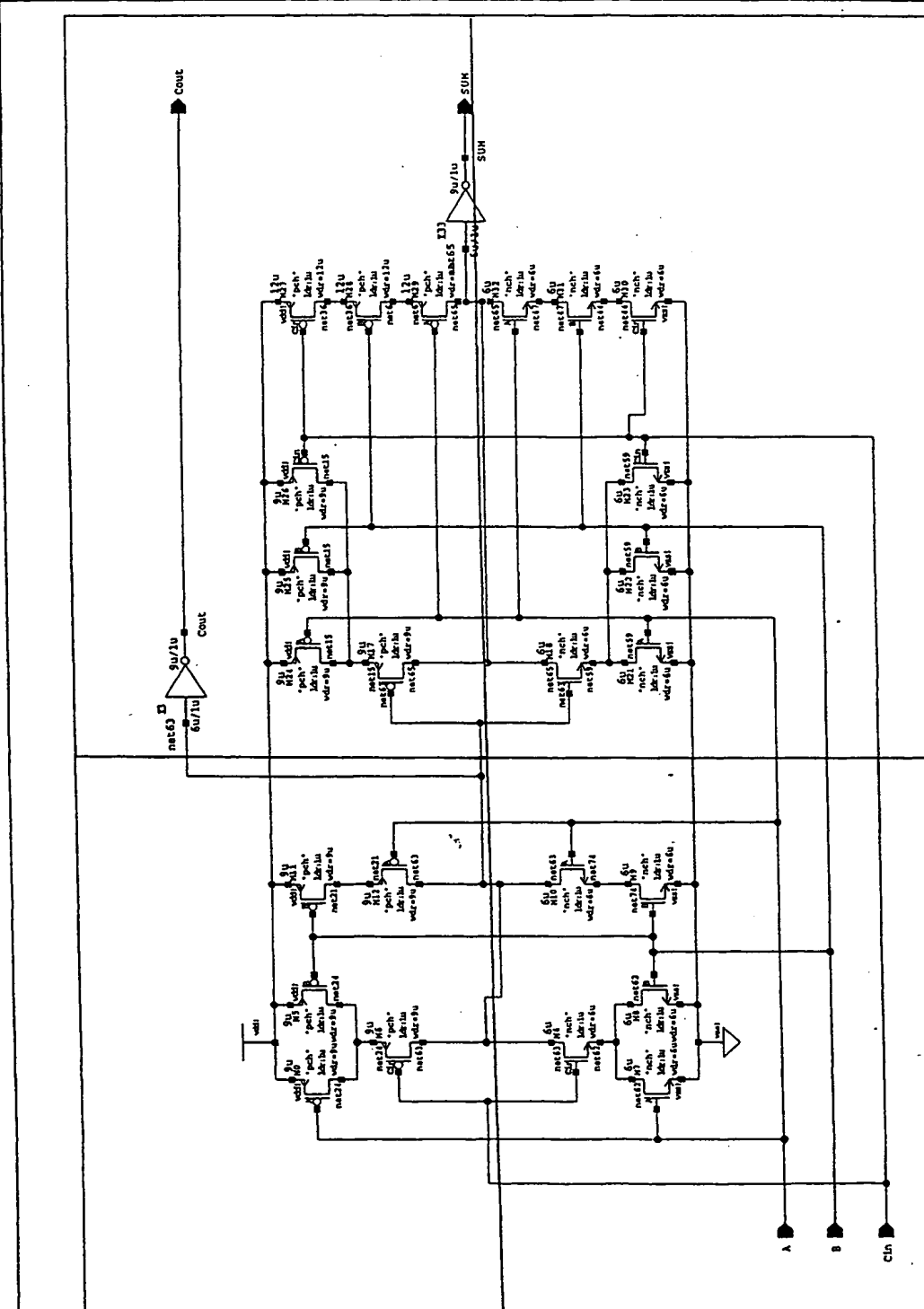
8.0203AA	8.0203AB	8.0203AC
8.0203BA	8.0203BB	8.0203BC

EE 88.002003



8.020301AA	8.020301AB
8.020301BA	8.020301BB

II II 8.020301



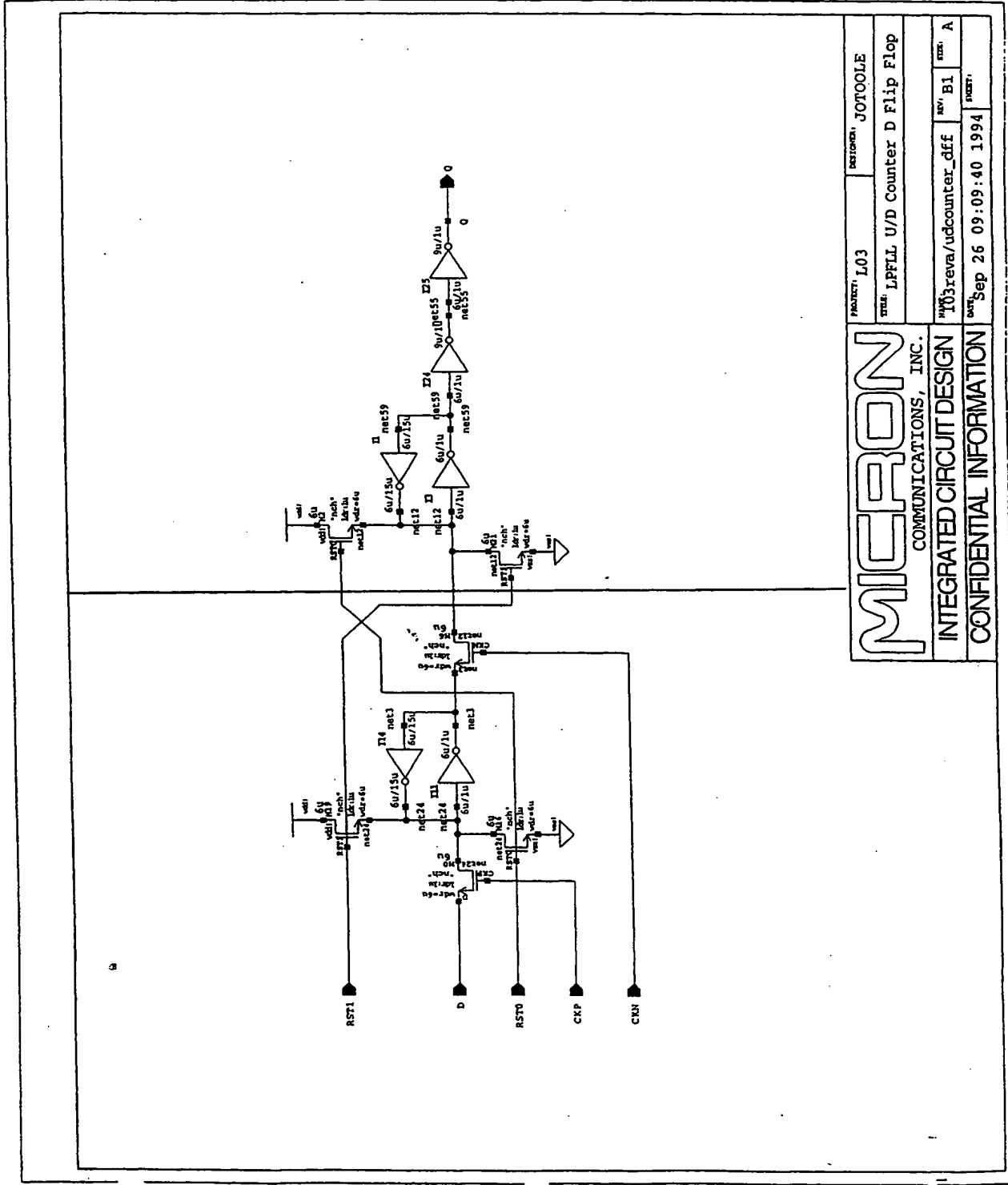
MICRON		COMMUNICATIONS, INC.	
PROJECT: L03		DESIGNED: JOTOOLE	
TITLE: UD Counter Adder			
INTEGRATED CIRCUIT DESIGN: jfreva/udcounter_adder		REV: B1	SIZE: A
CONFIDENTIAL INFORMATION		DATE: Sep 26 09:08:56 1994	

Fig. 8.020501

8.020302AB

8.020302AA

8.020302



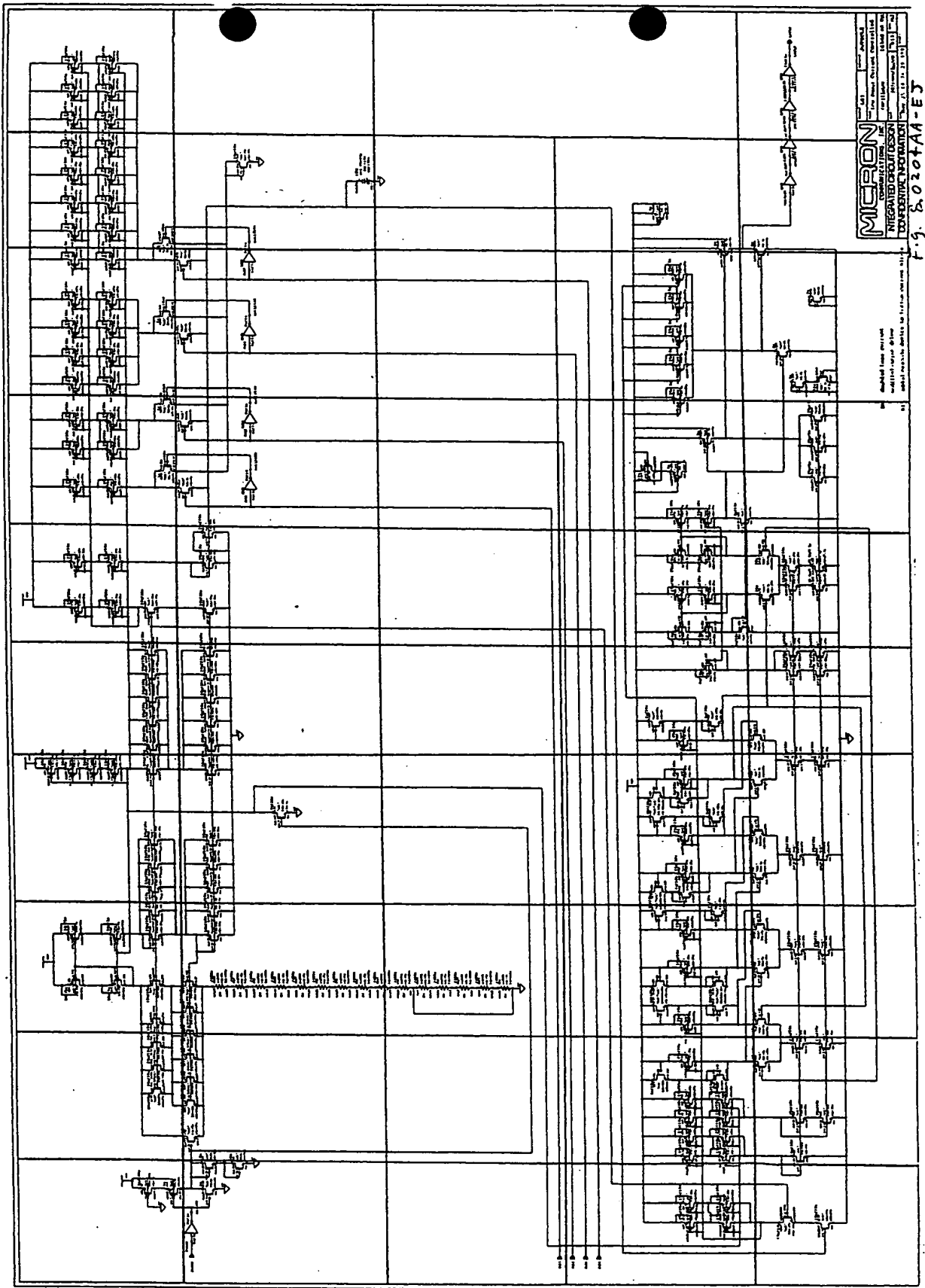
<b>MICRON</b>		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: LPFLL U/D Counter D Flip Flop	
INTEGRATED CIRCUIT DESIGN		PART: T03reva/udcounter_dff	
CONFIDENTIAL INFORMATION		REV: B1	REV: A
		DATE: Sep 26 09:09:40 1994	

Fig. 8.020302

8.0204AA	8.0204AB	8.0204AC	8.0204AD	8.0204AE	8.0204AF	8.0204AG	8.0204AH	8.0204AI	8.0204AJ
8.0204BA	8.0204BB	8.0204BC	8.0204BD	8.0204BE	8.0204BF	8.0204BG	8.0204BH	8.0204BI	8.0204BJ
8.0204CA	8.0204CB	8.0204CC	8.0204CD	8.0204CE	8.0204CF	8.0204CG	8.0204CH	8.0204CI	
8.0204DA	8.0204DB	8.0204DC	8.0204DD	8.0204DE	8.0204DF	8.0204DG	8.0204DH	8.0204DI	
8.0204EA	8.0204EB	8.0204EC	8.0204ED	8.0204EE	8.0204EF	8.0204EG	8.0204EH	8.0204EI	8.0204EJ

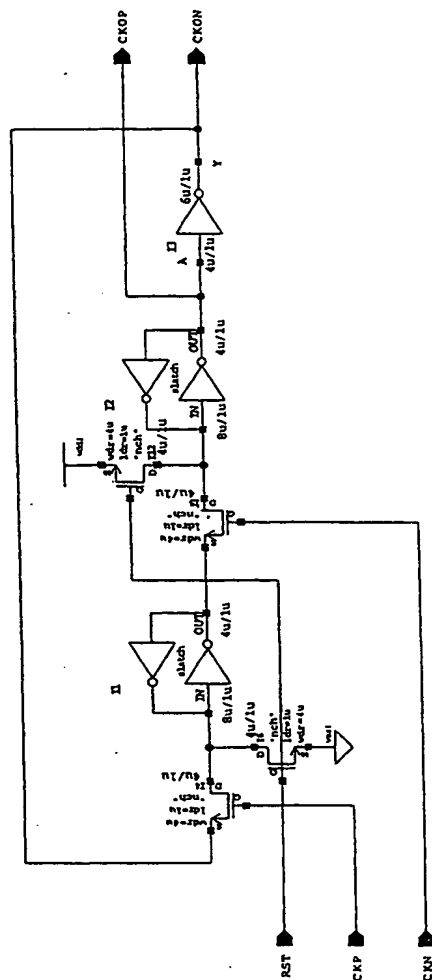
1902.8.15





**MICRON**  
INTEGRATED CIRCUIT DESIGN  
EXPERIMENTAL INFORMATION  
Part 80204AA-E3

Fig. 80204AA-E3



12/29/92

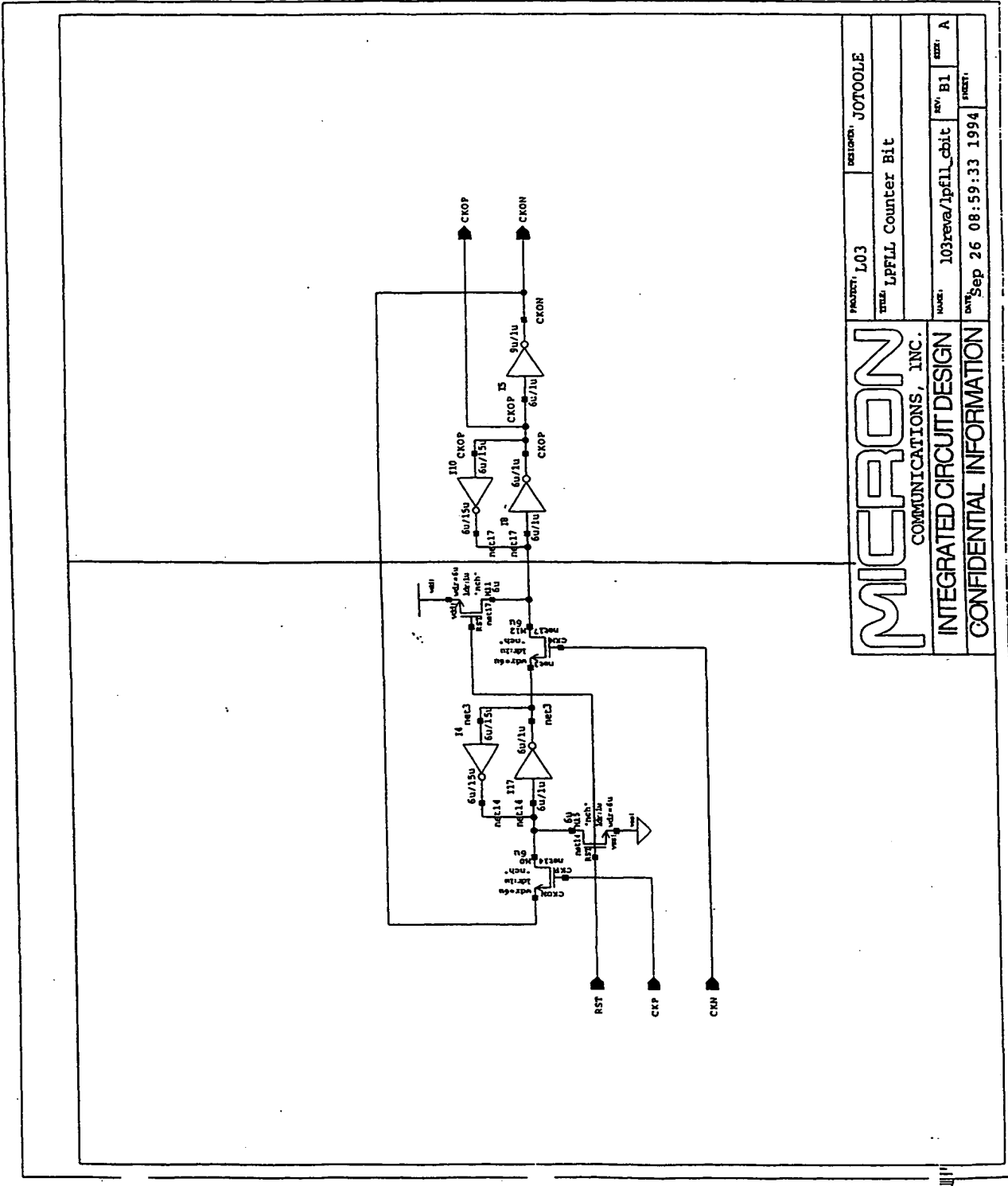
PROJECT: L03		SECTION: Ratcoll
TITLE: Titled Lockout Divider Call		
NAME:	103rev/a/1/d/c/d	REV: A
DATE: Sep 22 15:26:56 1994		SHEET:

8.03AB

8.03AA

LEWIS & CLARK

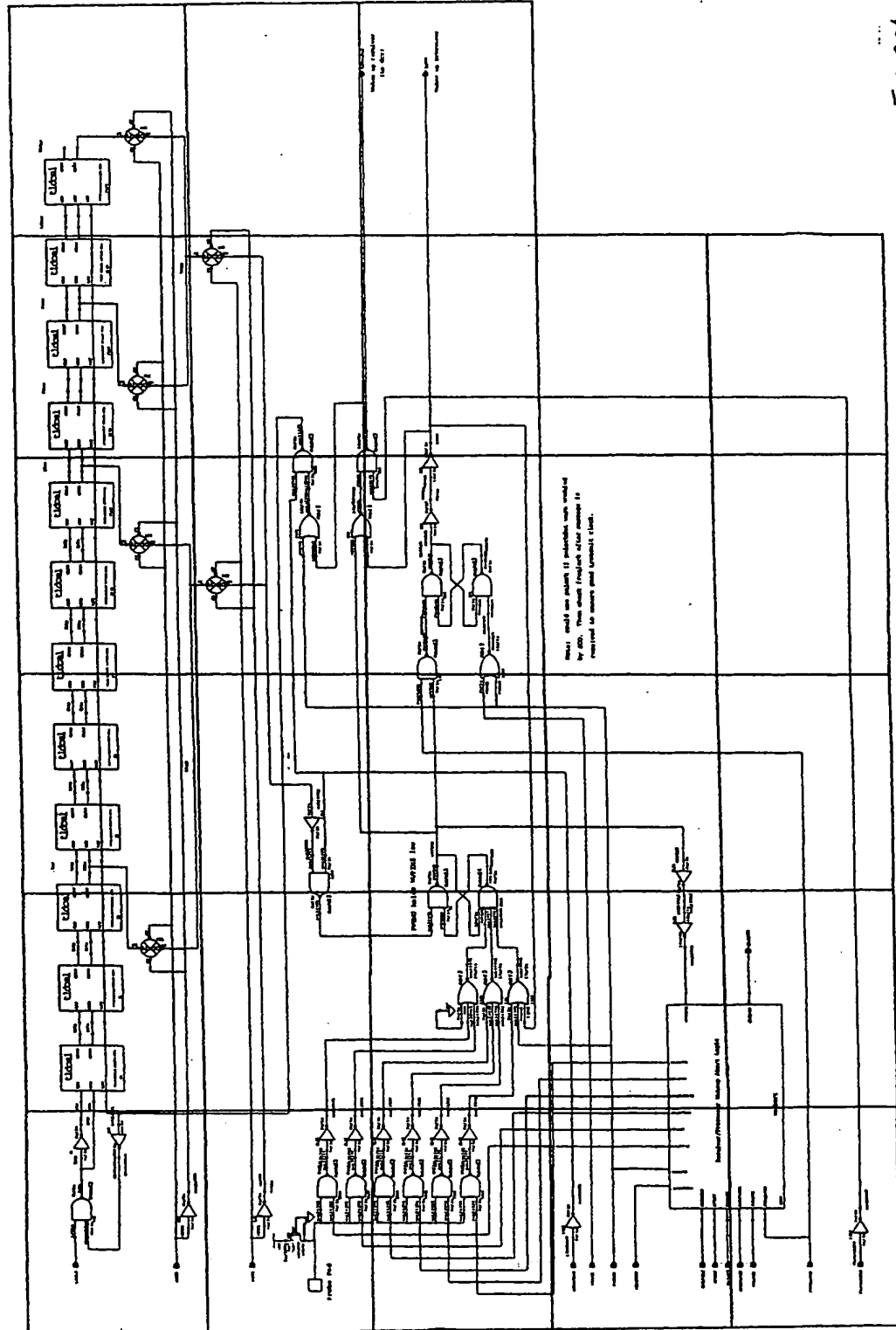
FIG. 8.03



MICRON		PROPERTY: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: LPFLL Counter Bit	
INTEGRATED CIRCUIT DESIGN		DATE: 103revs/lpfill_cbit	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 26 08:59:33 1994	REV: A

8.04AA	8.04AB	8.04AC	8.04AD	8.04AE	8.04AF
8.04BA	8.04BB	8.04BC	8.04BD	8.04BE	8.04BF
8.04CA	8.04CB	8.04CC	8.04CD	8.04CE	8.04CF
8.04DA	8.04DB	8.04DC	8.04DD	8.04DE	
8.04EA	8.04EB	8.04EC	8.04ED	8.04EE	

EE BB.0000



(Indica el punto de partida)

Bill, and just led me through the house. I was surprised to find the

**NOTED**

1. The following information is required for the purpose of the investigation:

<b>MICRON</b>		CONSULTATIONS, INC.	
INTEGRATED CIRCUIT DESIGN			
CONFIDENTIAL INFORMATION			
DATE	10-1	101 pages / pages	711
DATE	10-1	10-10-83	10-1

8.0401AA	8.0401AB	8.0401AC	8.0401AD	8.0401AE
8.0401BA	8.0401BB	8.0401BC	8.0401BD	8.0401BE
8.0401CA	8.0401CB	8.0401CC	8.0401CD	8.0401CE
8.0401DA	8.0401DB	8.0401DC	8.0401DD	8.0401DE

II II II II II II

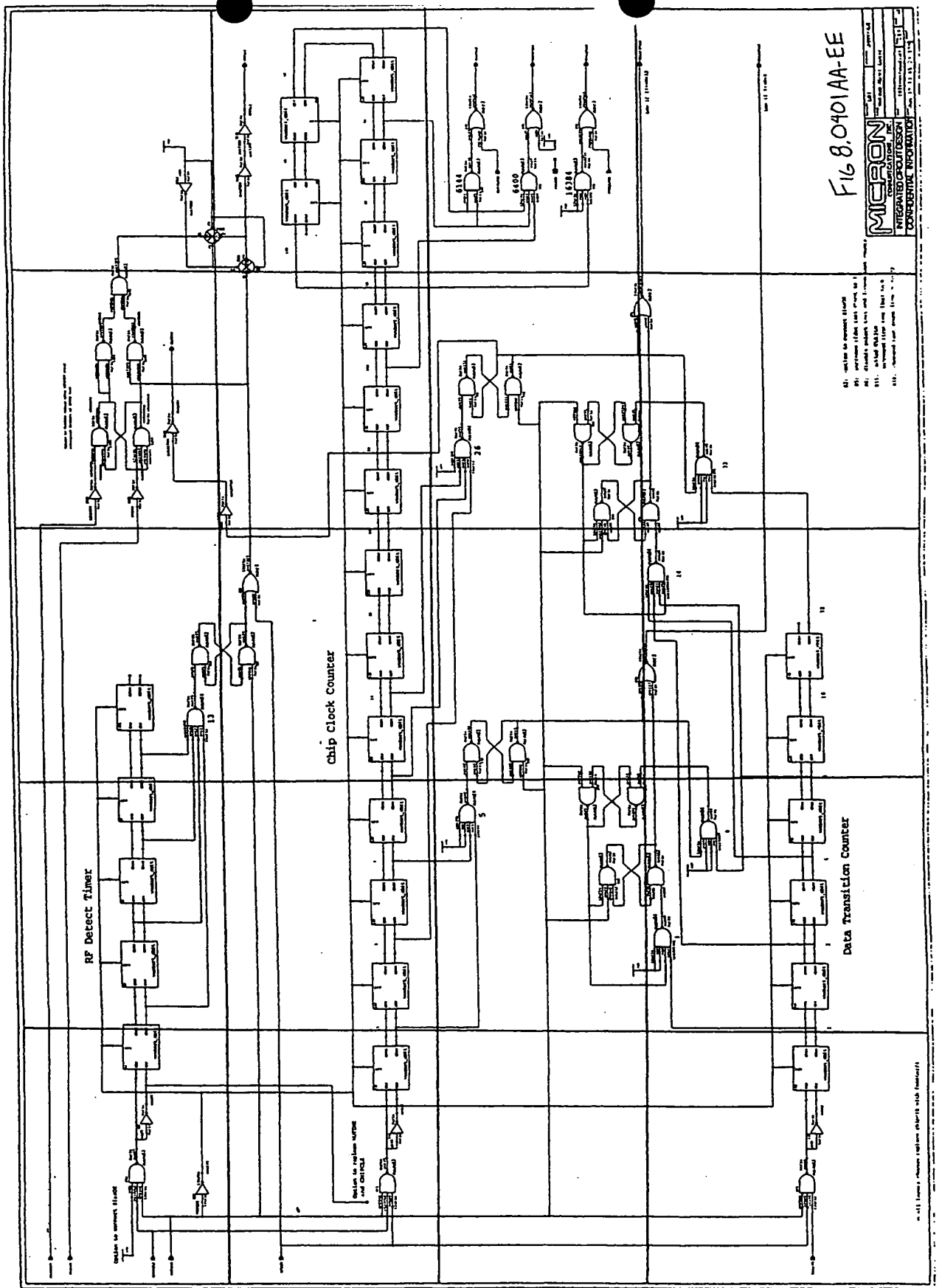


FIG 8.0401AA-EE

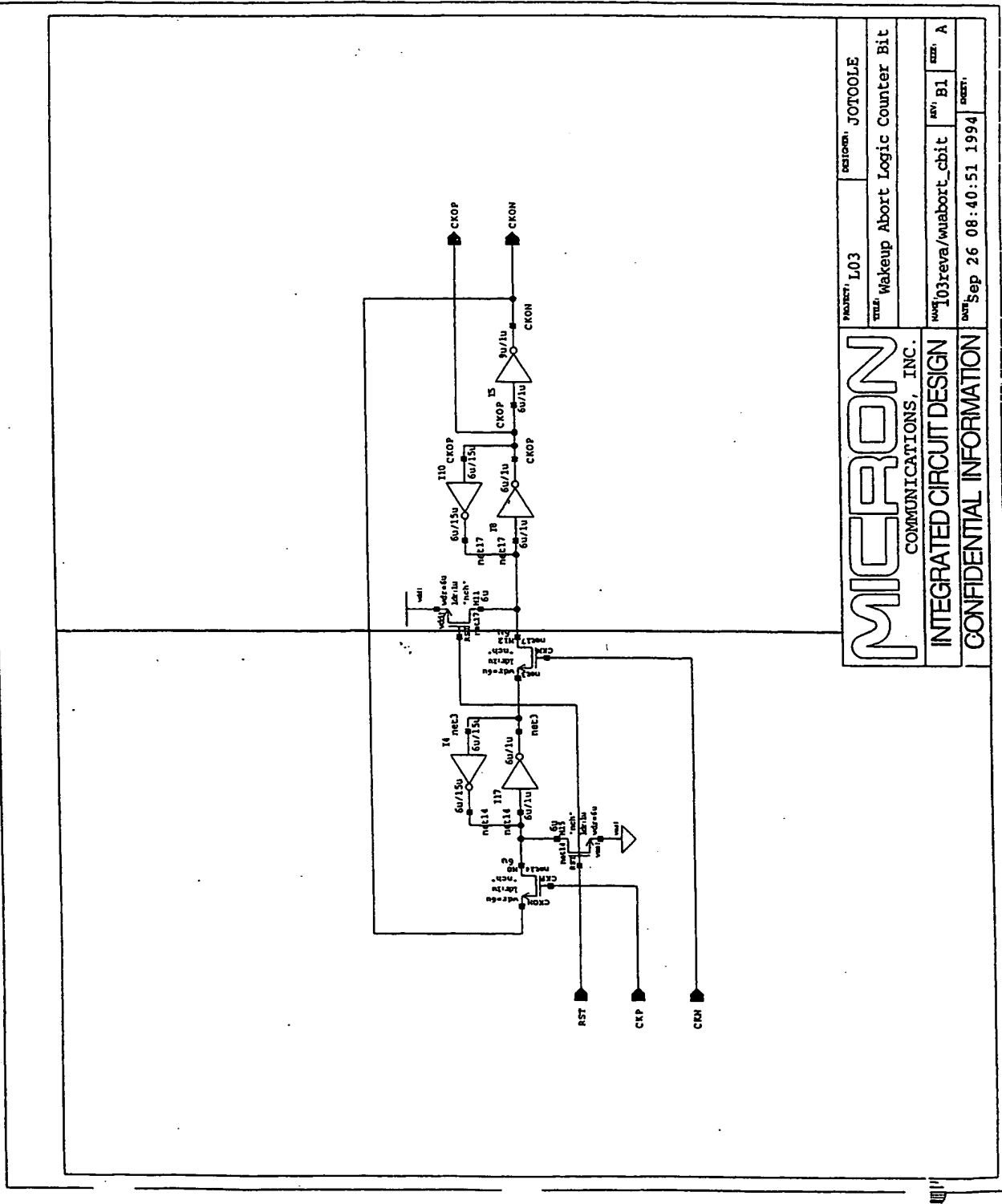
**MICRON**  
 INTEGRATED CIRCUITS  
 CONFIDENTIAL INFORMATION

- 81. option to support filter
- 82. option to filter out error
- 83. option to filter out error
- 84. option to filter out error
- 85. option to filter out error
- 86. option to filter out error
- 87. option to filter out error
- 88. option to filter out error
- 89. option to filter out error
- 90. option to filter out error
- 91. option to filter out error
- 92. option to filter out error
- 93. option to filter out error
- 94. option to filter out error
- 95. option to filter out error
- 96. option to filter out error
- 97. option to filter out error
- 98. option to filter out error
- 99. option to filter out error
- 100. option to filter out error



**8.040101AA**

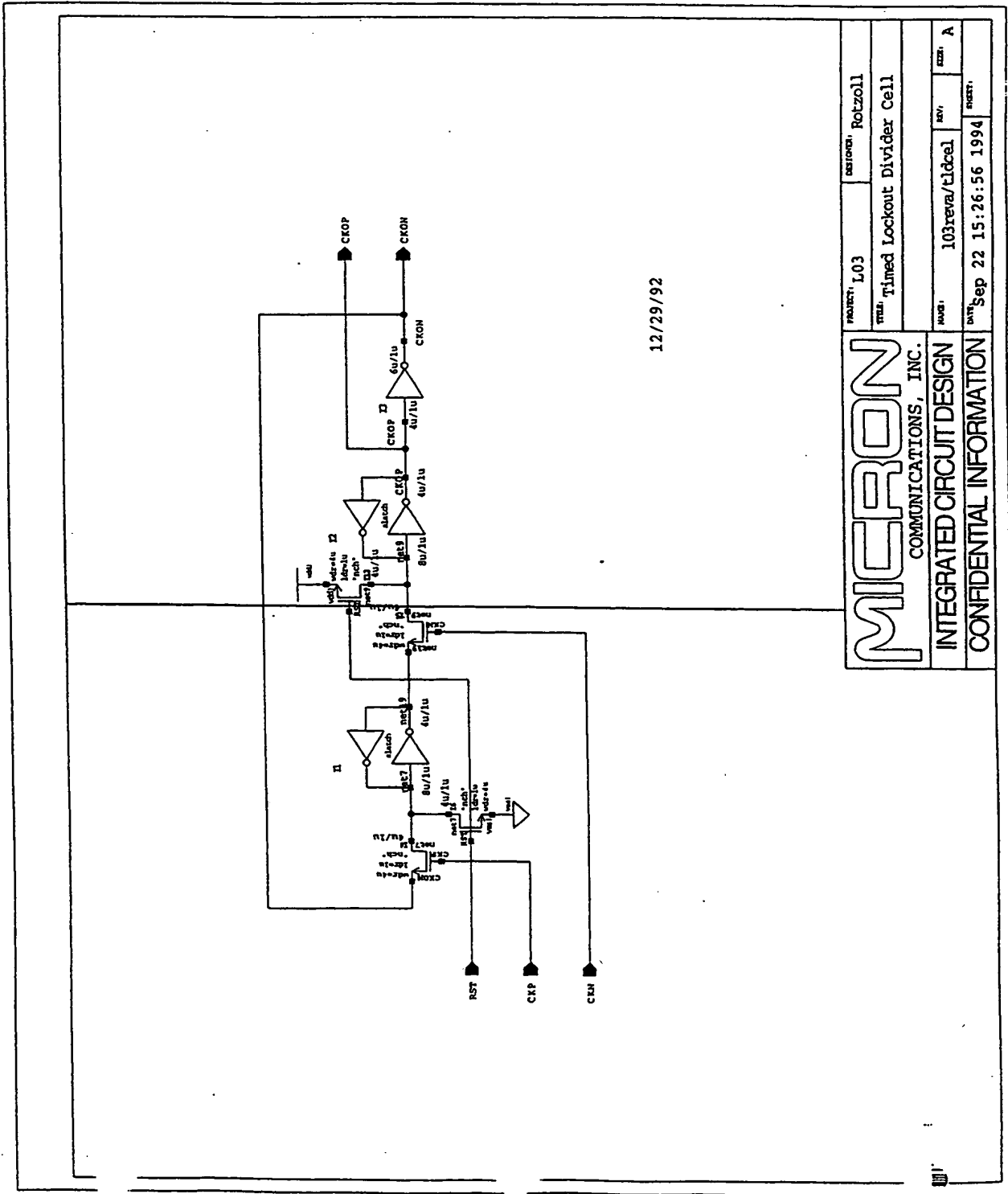
[illegible]



MICRON		DESIGN: JOTOOLE
COMMUNICATIONS, INC.		PROJECT: L03
INTEGRATED CIRCUIT DESIGN		TITLE: Wakeup Abort Logic Counter Bit
CONFIDENTIAL INFORMATION		DATE: 103revA/wuabort_cbit
		REV: B1
		DATE: Sep 26 08:40:51 1994
		DESIGN: A

8.0402AA	8.0402AB
----------	----------

EX-88.0402

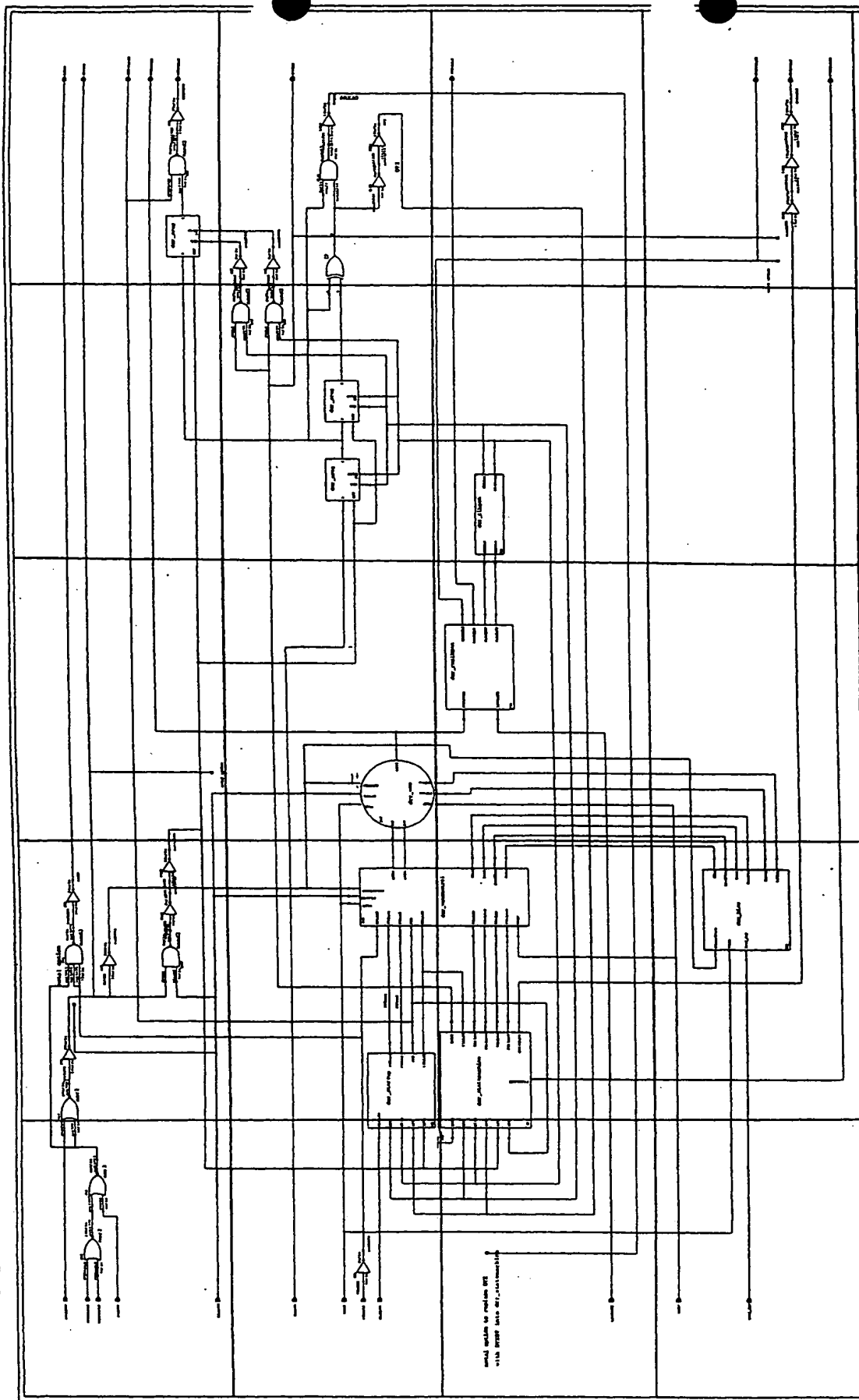


MICRON		PROJECT: L03	DESIGNER: Rotzoll
COMMUNICATIONS, INC.		TITLE: Timed Lockout Divider Cell	
INTEGRATED CIRCUIT DESIGN		AUG: 103reva/tldcel	
CONFIDENTIAL INFORMATION		DATE: Sep 22 15:26:56 1994	DESIGN: A

FIG. 8.0402

8.05AA	8.05AB	8.05AC	8.05AD	8.05AE
8.05BA	8.05BB	8.05BC	8.05BD	8.05BE
8.05CA	8.05CB	8.05CC	8.05CD	8.05CE
8.05DA	8.05DB	8.05DC	8.05DD	8.05DE

EX-88.005



M1: defined from logic  
 M2: defined from logic  
 M3: defined from logic  
 M4: defined from logic  
 M5: defined from logic  
 M6: defined from logic  
 M7: defined from logic  
 M8: defined from logic  
 M9: defined from logic  
 M10: defined from logic  
 M11: defined from logic  
 M12: defined from logic  
 M13: defined from logic  
 M14: defined from logic  
 M15: defined from logic  
 M16: defined from logic  
 M17: defined from logic  
 M18: defined from logic  
 M19: defined from logic  
 M20: defined from logic  
 M21: defined from logic  
 M22: defined from logic  
 M23: defined from logic  
 M24: defined from logic  
 M25: defined from logic  
 M26: defined from logic  
 M27: defined from logic  
 M28: defined from logic  
 M29: defined from logic  
 M30: defined from logic  
 M31: defined from logic  
 M32: defined from logic  
 M33: defined from logic  
 M34: defined from logic  
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 M36: defined from logic  
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 M73: defined from logic  
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 M76: defined from logic  
 M77: defined from logic  
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 M87: defined from logic  
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 M89: defined from logic  
 M90: defined from logic  
 M91: defined from logic  
 M92: defined from logic  
 M93: defined from logic  
 M94: defined from logic  
 M95: defined from logic  
 M96: defined from logic  
 M97: defined from logic  
 M98: defined from logic  
 M99: defined from logic  
 M100: defined from logic

Fig. 8.05

**MICRON**  
 CORPORATION  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION  
 10000 NE 28th Ave., Portland, OR 97210  
 (503) 253-1000  
 1980

8.0501AA	8.0501AB	8.0501AC	8.0501AD	8.0501AE
8.0501BA	8.0501BB	8.0501BC	8.0501BD	8.0501BE

BB.0500.11

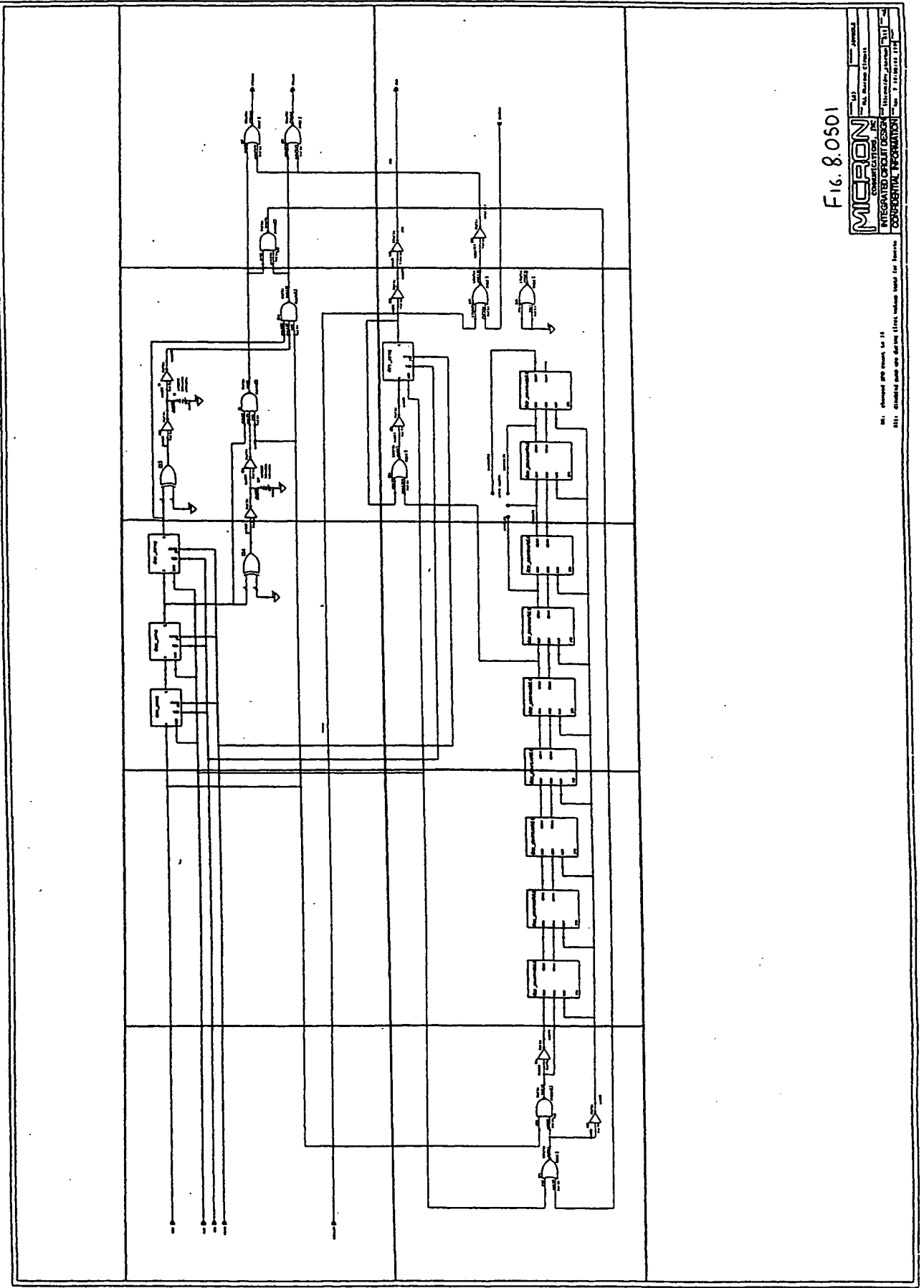


FIG. 8.0501

MICRON	
INTEGRATED CIRCUIT DESIGN	CONFIDENTIAL INFORMATION
DATE: 10/10/81	DESIGNER: J. J. J.
REVISION: 1	REVISION: 1

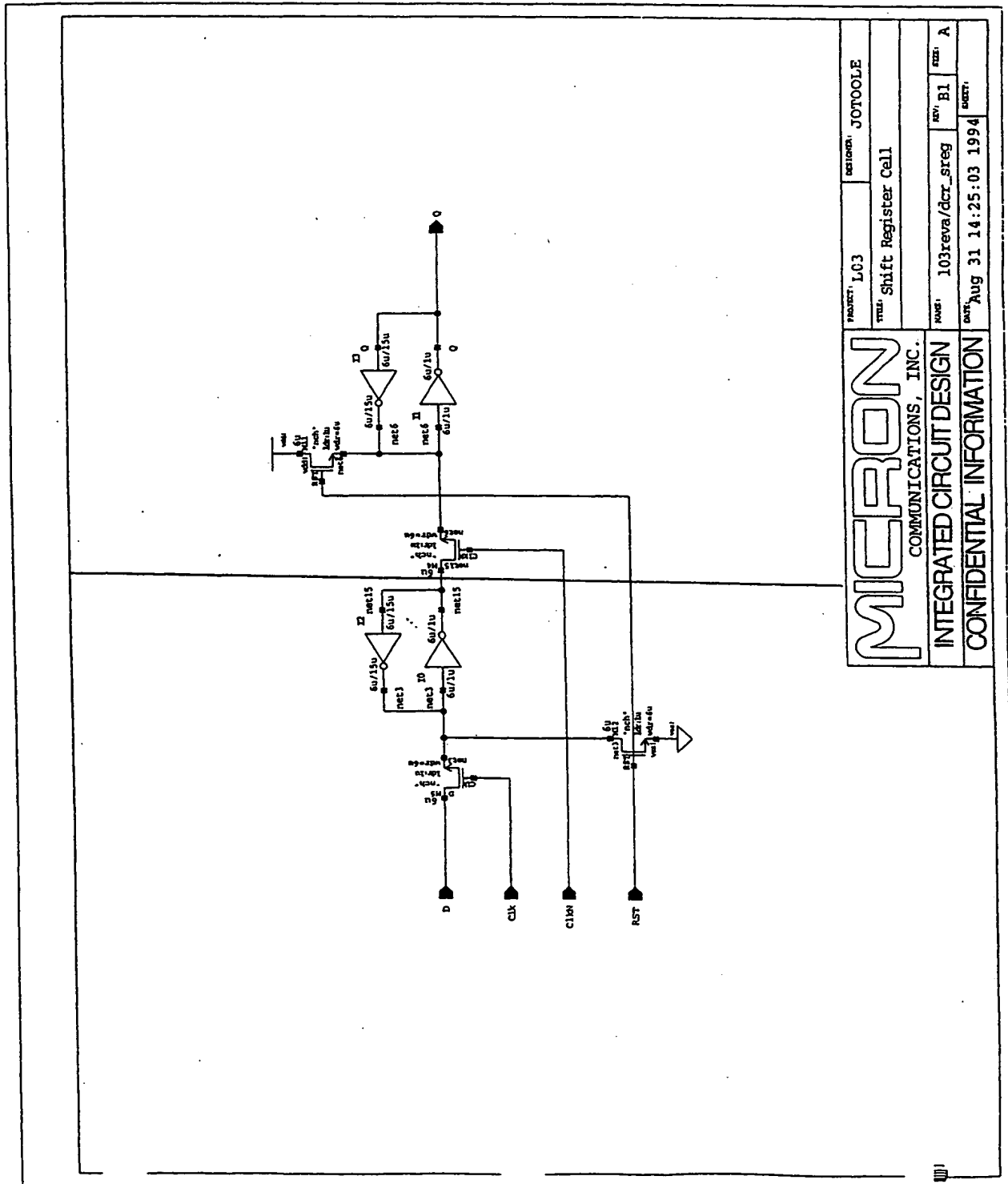
NOT: Observed and tested in 10  
 101: Observed and tested in 10



8.050101AB

8.050101AA

IL 50 50 101 101



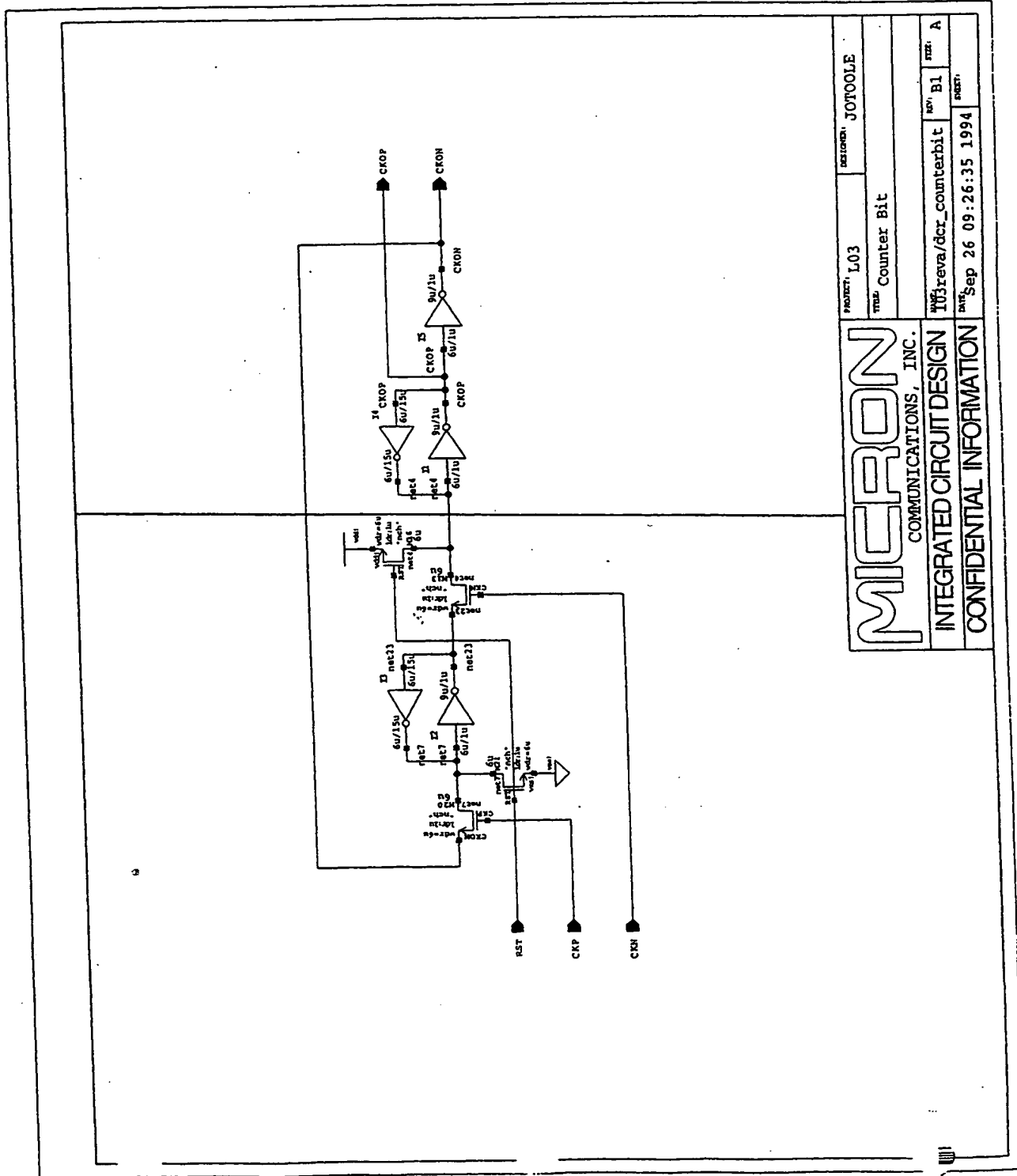
MICRON		PRODUCT: LC3	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Shift Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/dcr_sreg	REV: B1
CONFIDENTIAL INFORMATION		DATE: Aug 31 14:25:03 1994	SIZE: A

FIG. 8.050101

8.050102AB

8.050102AA

EX-88-050102



MICRON		PRODUCT: L03	REVISION: J0700LE
COMMUNICATIONS, INC.		Title: Counter Bit	
INTEGRATED CIRCUIT DESIGN		REV: B1	SIZE: A
CONFIDENTIAL INFORMATION		DATE: Sep 26 09:26:35 1994	DESIGN

FIG. 8.050102

8.0502AA	8.0502AB	8.0502AC	8.0502AD
8.0502BA	8.0502BB	8.0502BC	8.0502BD
8.0502CA	8.0502CB	8.0502CC	8.0502CD

II II II II II II II II

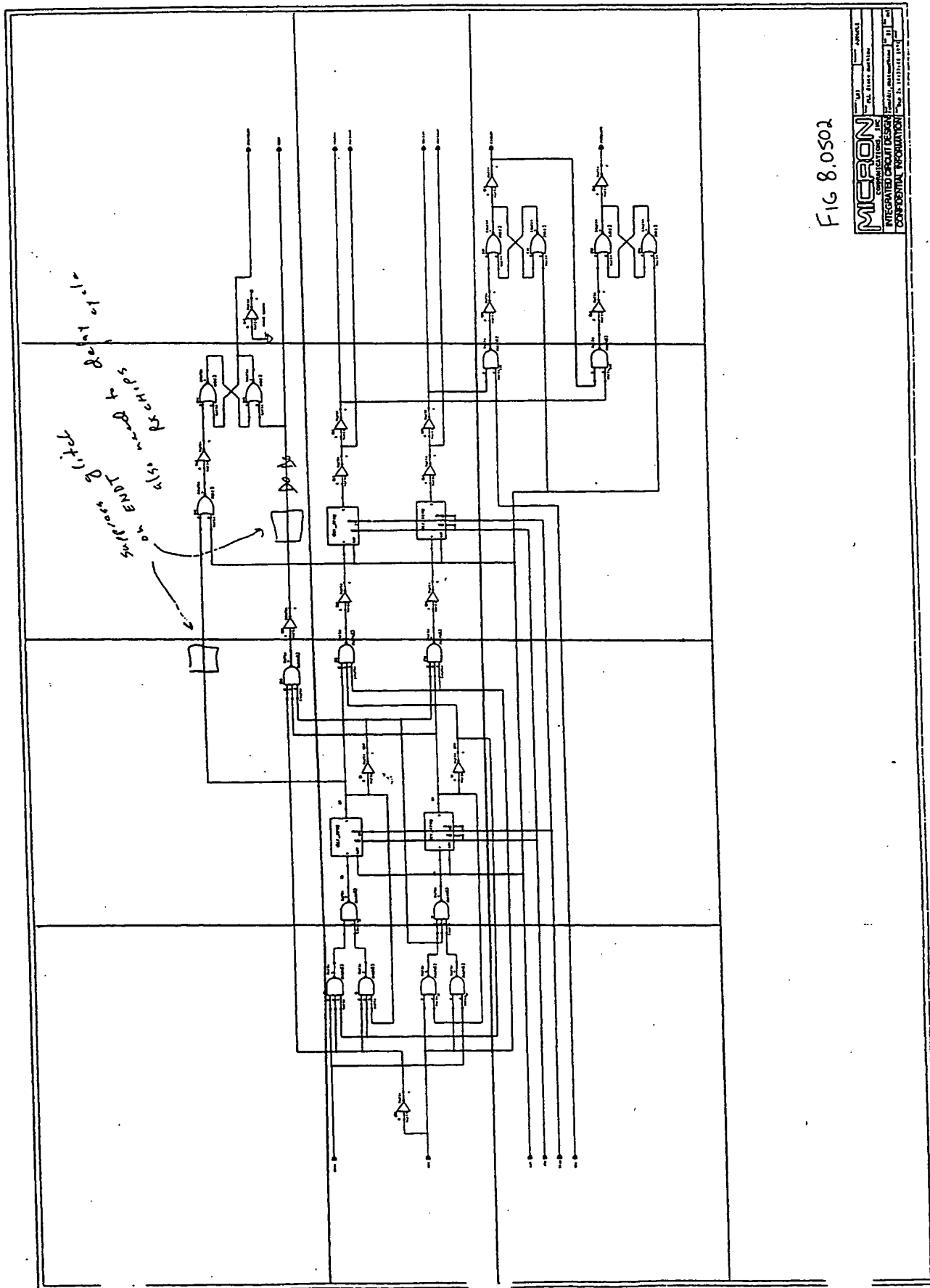
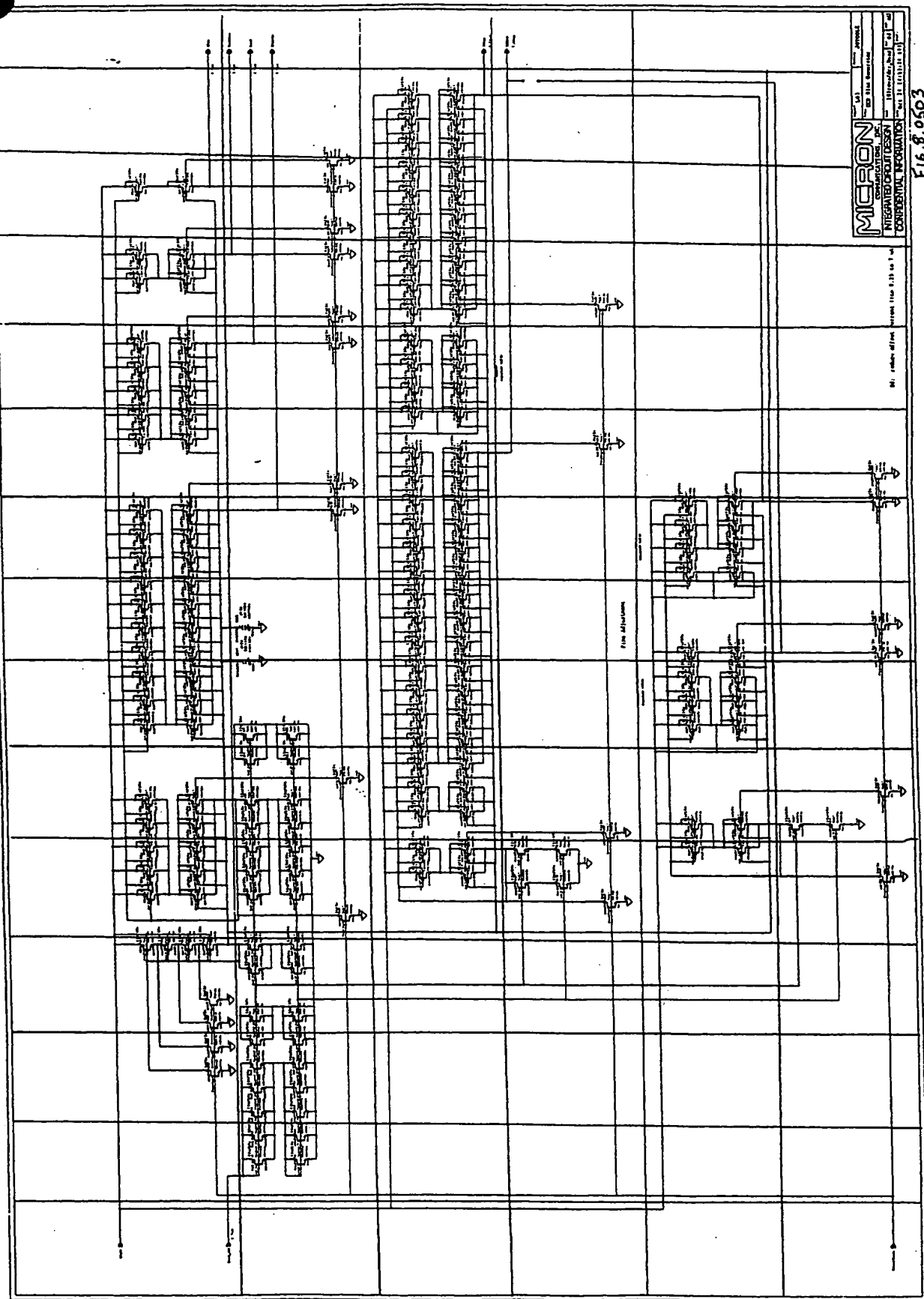


Fig 8.0502

8.05034A	8.05034B	8.05034C	8.05034D	8.05034E	8.05034F	8.05034G	8.05034H	8.05034I	8.05034J	8.05034K	8.05034L	8.05034M	8.05034N	8.05034O
8.05038A	8.05038B	8.05038C	8.05038D	8.05038E	8.05038F	8.05038G	8.05038H	8.05038I	8.05038J	8.05038K	8.05038L	8.05038M	8.05038N	8.05038O
8.0503CA	8.0503CB	8.0503CC	8.0503CD	8.0503CE	8.0503CF	8.0503CG	8.0503CH	8.0503CI	8.0503CJ	8.0503CK	8.0503CL	8.0503CM	8.0503CN	8.0503CO
8.0503DA	8.0503DB	8.0503DC	8.0503DD	8.0503DE	8.0503DF	8.0503DG	8.0503DH	8.0503DI	8.0503DJ	8.0503DK	8.0503DL	8.0503DM	8.0503DN	8.0503DO
8.0503EA	8.0503EB	8.0503EC	8.0503ED	8.0503EE	8.0503EF	8.0503EG	8.0503EH	8.0503EI	8.0503EJ	8.0503EK	8.0503EL	8.0503EM	8.0503EN	
8.0503FA	8.0503FB	8.0503FC	8.0503FD	8.0503FE	8.0503FF	8.0503FG	8.0503FH	8.0503FI	8.0503FJ	8.0503FK	8.0503FL	8.0503FM	8.0503FN	

DEPARTMENT OF DEFENSE

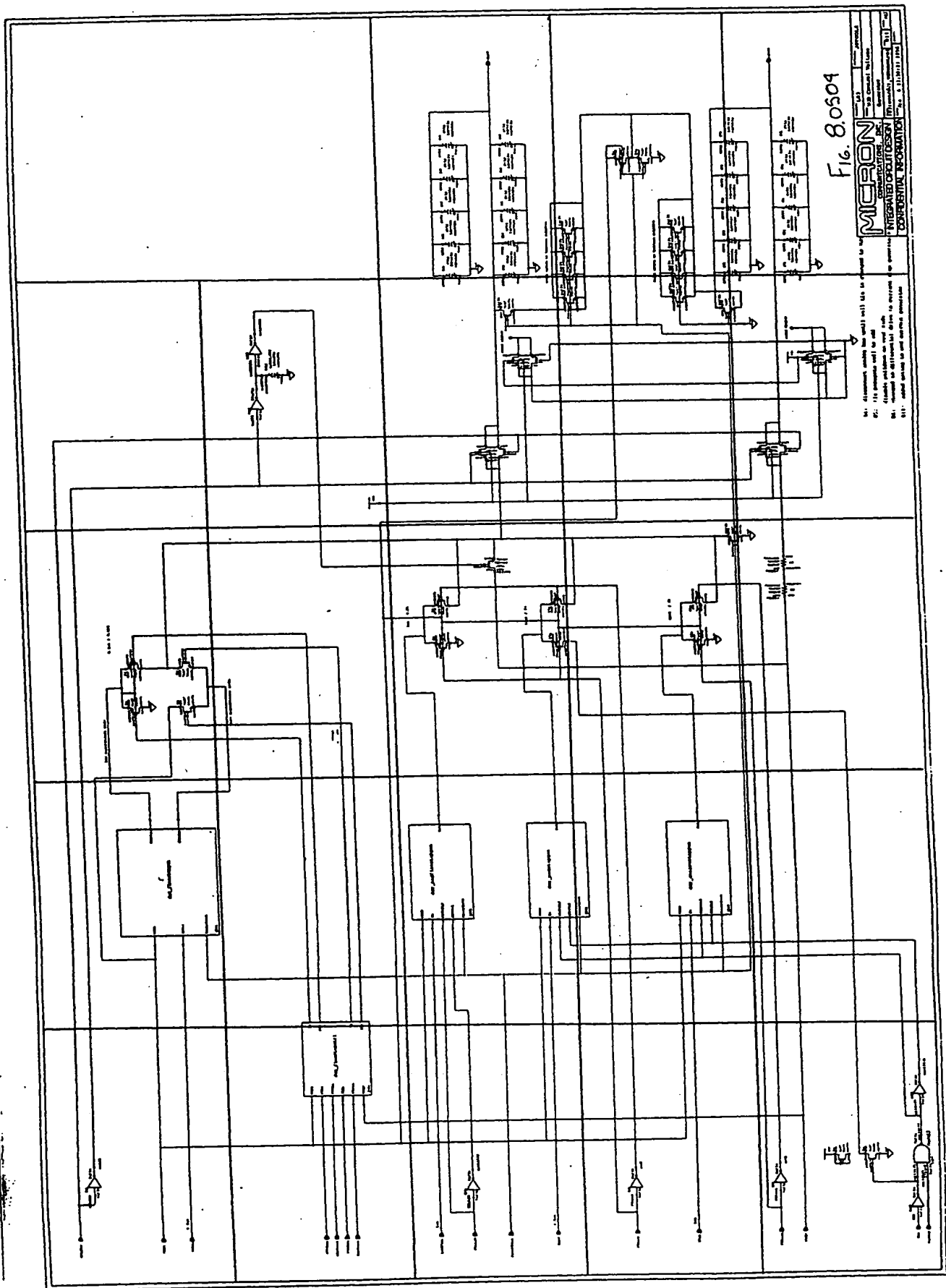
Fig. 8.0603





8.0504AA	8.0504AB	8.0504AC	8.0504AD	
8.0504BA	8.0504BB	8.0504BC	8.0504BD	
8.0506CA	8.0504CB	8.0504CC	8.0504CD	8.0504CE
8.0504DA	8.0504DB	8.0504DC	8.0504DD	8.0504DE
8.0504EA	8.0504EB	8.0504EC	8.0504ED	8.0504EE

EEB.0504



8.050401AA	8.050401AB	8.050401AC	8.050401AD	8.050401AE	8.050401AF	8.050401AG	8.050401AH	8.050401AJ	
8.050401BA	8.050401BB	8.050401BC	8.050401BD	8.050401BE	8.050401BF	8.050401BG	8.050401BH	8.050401BJ	8.050401BK
8.050401CA	8.050401CB	8.050401CC	8.050401CD	8.050401CE	8.050401CF	8.050401CG	8.050401CH	8.050401CJ	8.050401CK

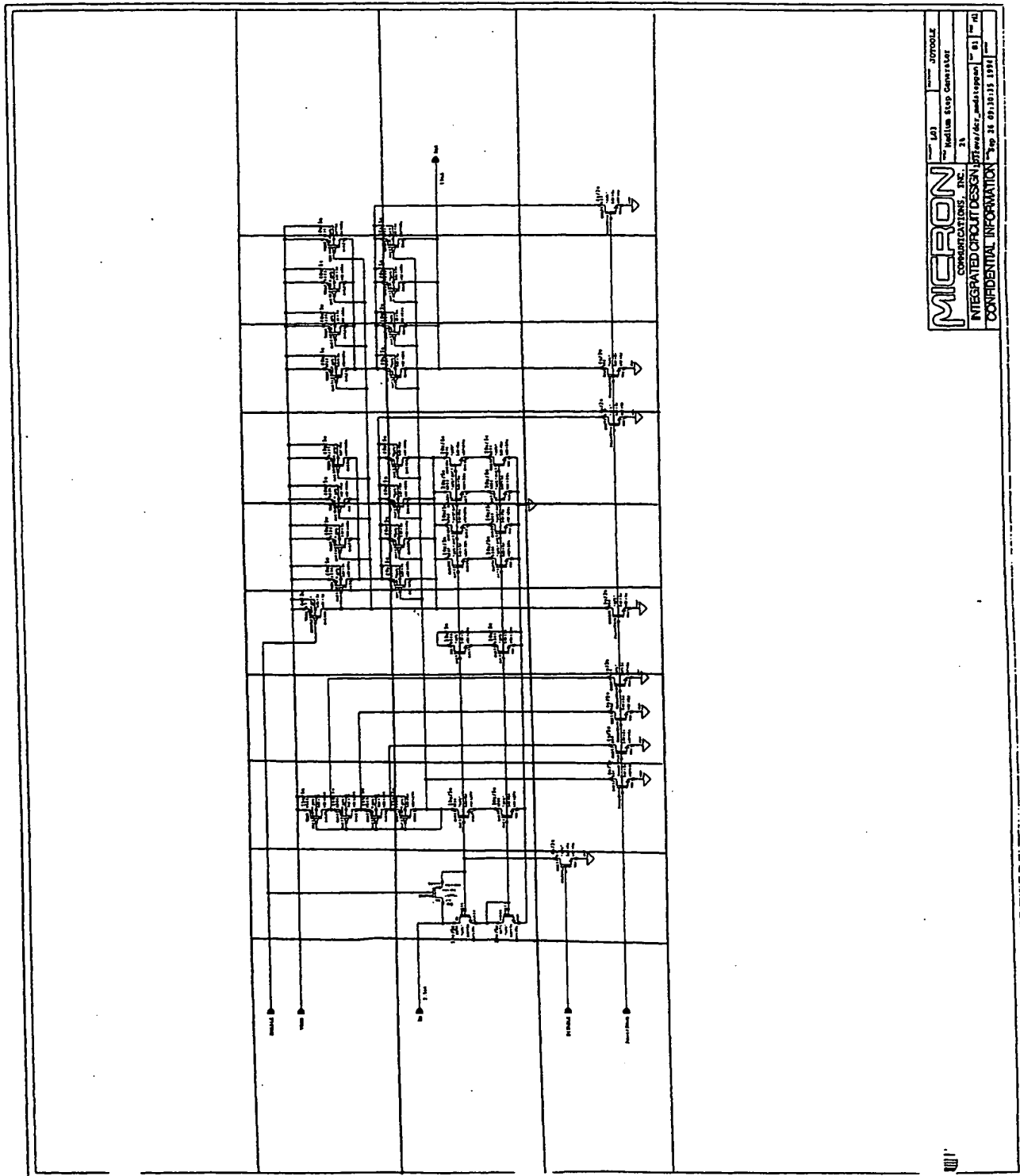
II II 8.050401



8.050402AA	8.050402AB	8.050402AC	8.050402AD	8.050402AE	8.050402AF	8.050402AG	8.050402AH	8.050402AI	8.050402AJ
8.050402BA	8.050402BB	8.050402BC	8.050402BD	8.050402BE	8.050402BF	8.050402BG	8.050402BH	8.050402BI	8.050402BJ
8.050402CA	8.050402CB	8.050402CC	8.050402CD	8.050402CE	8.050402CF	8.050402CG	8.050402CH	8.050402CI	8.050402CJ

8.050402

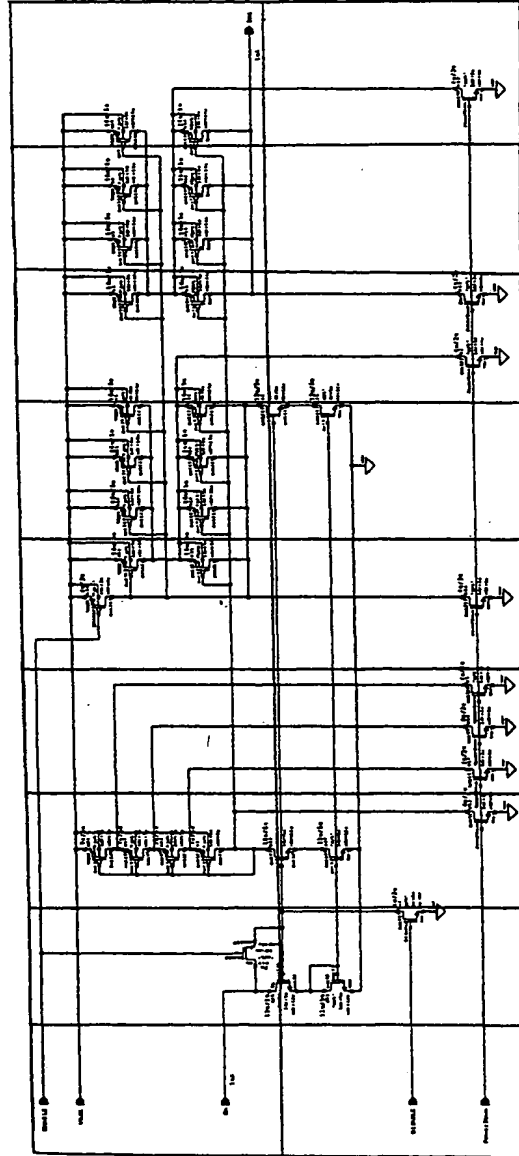
FIG. 8.050402



8.050403AA	8.050403AB	8.050403AC	8.050403AD	8.050403AE	8.050403AF	8.050403AG	8.050403AH	8.050403AI
8.050403BA	8.050403BB	8.050403BC	8.050403BD	8.050403BE	8.050403BF	8.050403BG	8.050403BH	8.050403BI

11 11 11 11 11 11 11 11 11

Fig. 8.050403

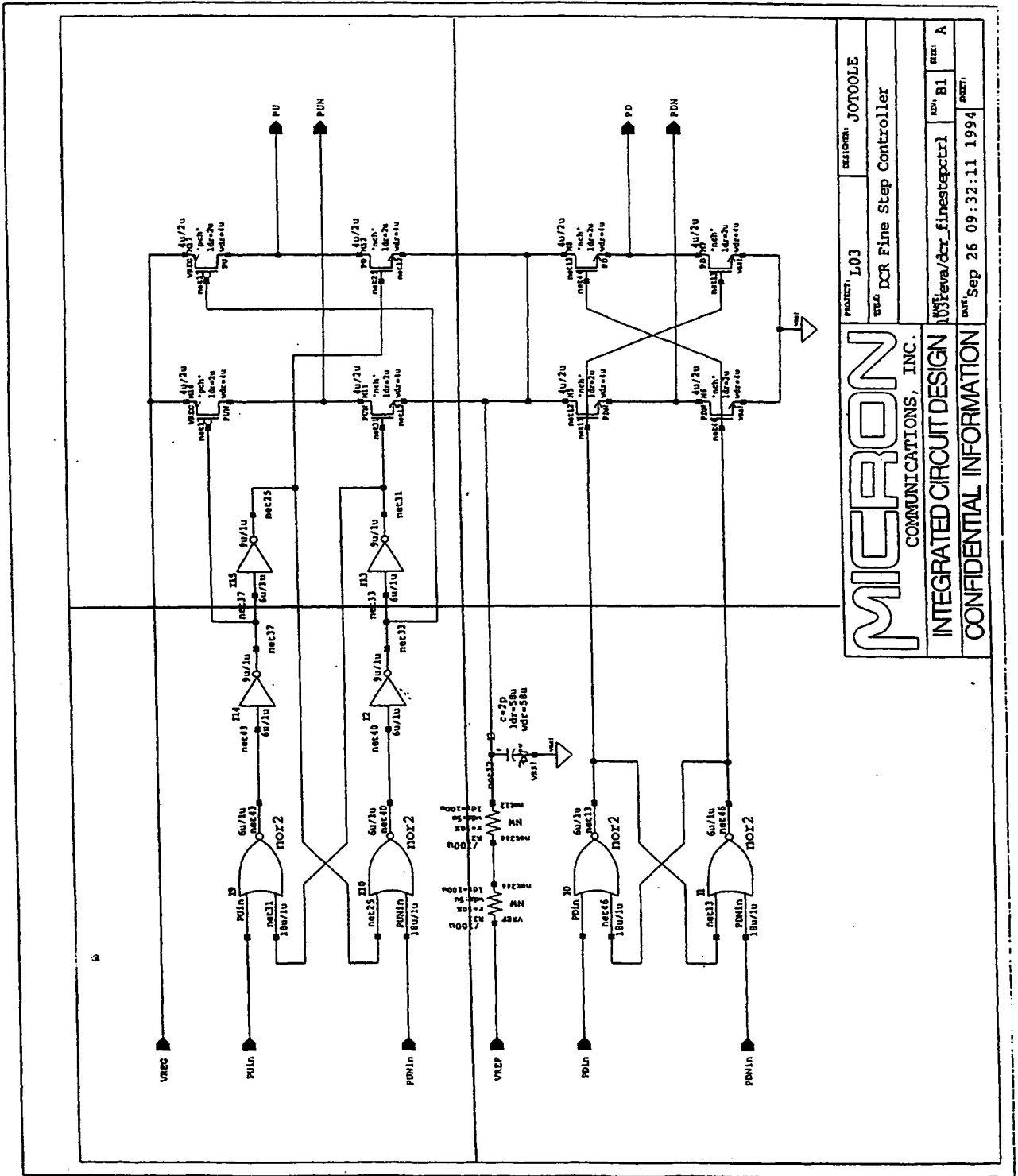


<b>MICRON</b>		U01	Jumpole
CONTRACT NO. 8.23		Medium Plane Strip Controller	
INTEGRATED CIRCUIT DESIGN		U01	U01
CONFIDENTIAL INFORMATION		Rev 26 09/11/18 1992	



8.050404AA	8.050404AB
8.050404BA	8.050404BB

EE B.050404A

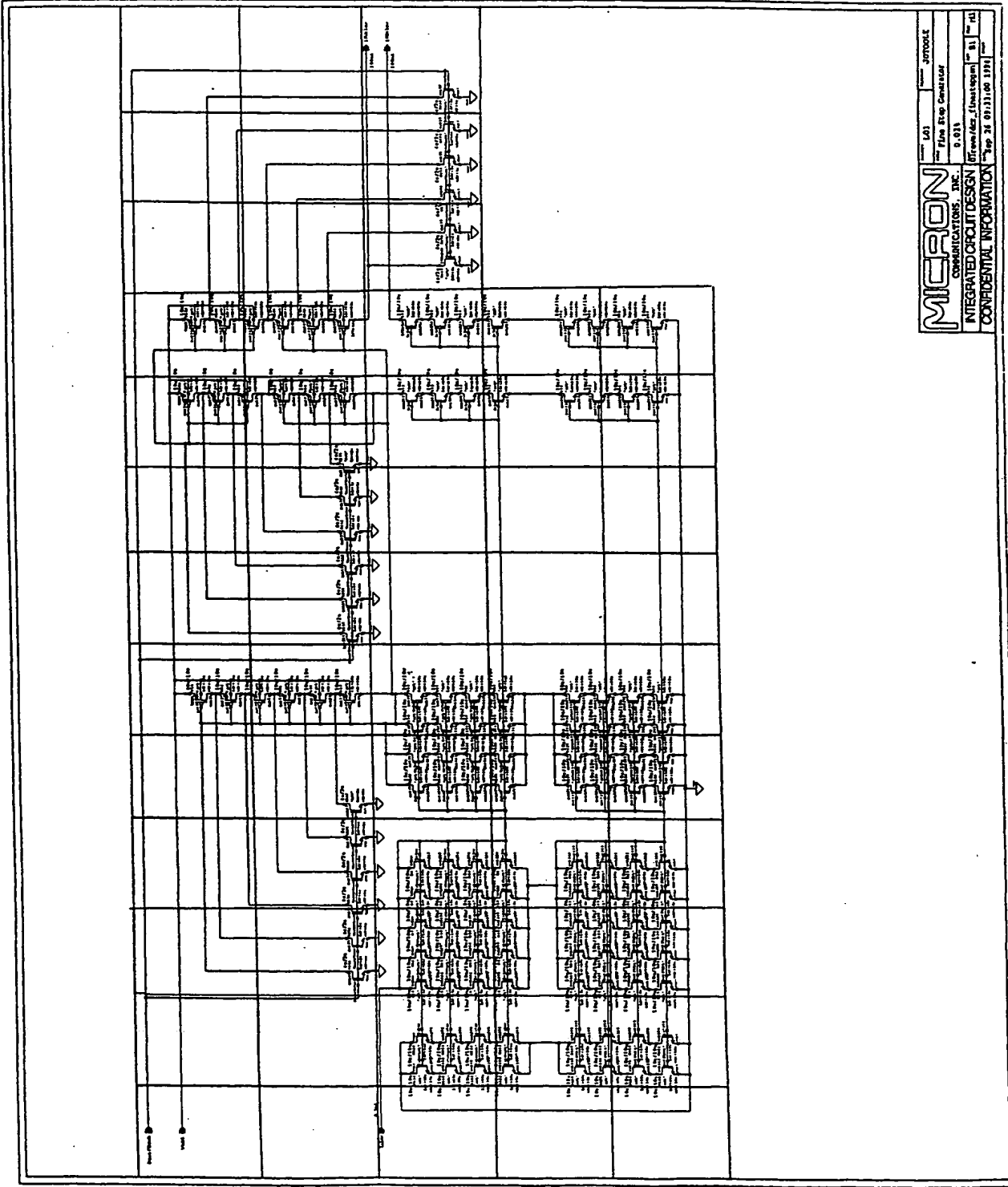


MICRON		PROJECT: L03	REVISION: J0700LE
COMMUNICATIONS, INC.		NAME: DCR Fine Step Controller	
INTEGRATED CIRCUIT DESIGN		DESIGNER: J0700LE	DATE: 26 09:32:11 1994
CONFIDENTIAL INFORMATION		REV: B1	SIZE: A

Fig. 8.050409

8.050405A	8.050405AB	8.050405AC	8.050405AD	8.050405AE	8.050405AF	8.050405AG	8.050405AH	8.050405AI	8.050405AJ	8.050405AK	8.050405AL	8.050405AM
8.050405BA	8.050405BB	8.050405BC	8.050405BD	8.050405BE	8.050405BF	8.050405BG	8.050405BH	8.050405BI	8.050405BJ	8.050405BK	8.050405BL	8.050405BM
8.050405CA	8.050405CB	8.050405CC	8.050405CD	8.050405CE	8.050405CF	8.050405CG	8.050405CH	8.050405CI	8.050405CJ	8.050405CK	8.050405CL	8.050405CM
8.050405DA	8.050405DB	8.050405DC	8.050405DD	8.050405DE	8.050405DF	8.050405DG	8.050405DH	8.050405DI	8.050405DJ			
8.050405EA	8.050405EB	8.050405EC	8.050405ED	8.050405EE	8.050405EF	8.050405EG	8.050405EH	8.050405EI	8.050405EJ			

IF II III IV V VI VII VIII IX X XI XII



**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

LAJ JETROSE  
Plan Step Controller  
0.011  
Frame Size (Unrotated) 11  
Top 24 01:31:00 1984

Fig 8.050405

8.05054A	8.05054B	8.05054C	8.05054D	8.05054E	8.05054F	8.05054G	8.05054H	8.05054I	8.05054J	8.05054K	8.05054L	8.05054M	8.05054N
8.0505BA	8.0505BB	8.0505BC	8.0505BD	8.0505BE	8.0505BF	8.0505BG	8.0505BH	8.0505BI	8.0505BJ	8.0505BK	8.0505BL	8.0505BM	8.0505BN
8.0505CA	8.0505CB	8.0505CC	8.0505CD	8.0505CE	8.0505CF	8.0505CG	8.0505CH	8.0505CI	8.0505CJ	8.0505CK	8.0505CL	8.0505CM	8.0505CN
8.0505DA	8.0505DB	8.0505DC	8.0505DD	8.0505DE	8.0505DF	8.0505DG	8.0505DH	8.0505DI	8.0505DJ	8.0505DK	8.0505DL	8.0505DM	8.0505DN
8.0505EA	8.0505EB	8.0505EC	8.0505ED	8.0505EE	8.0505EF								

JE II CS BB 0505

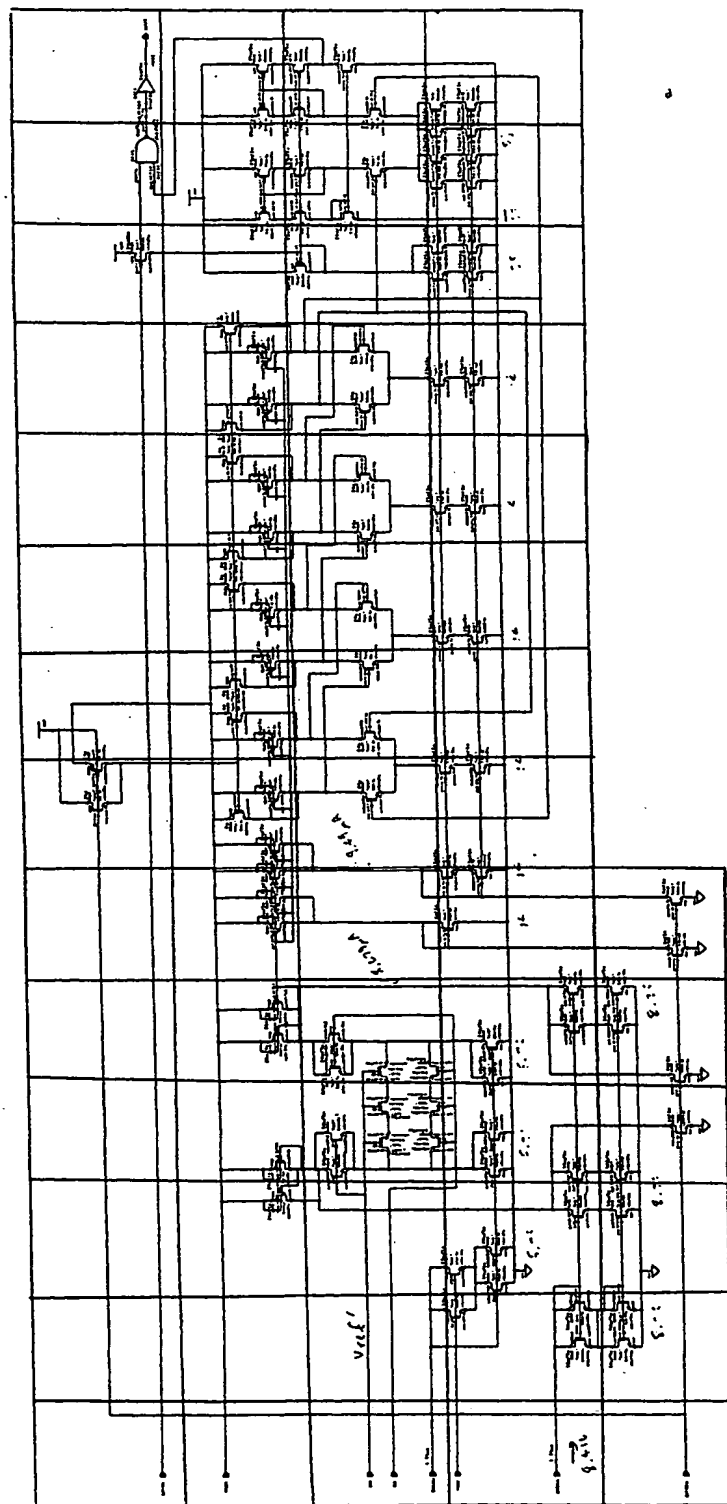


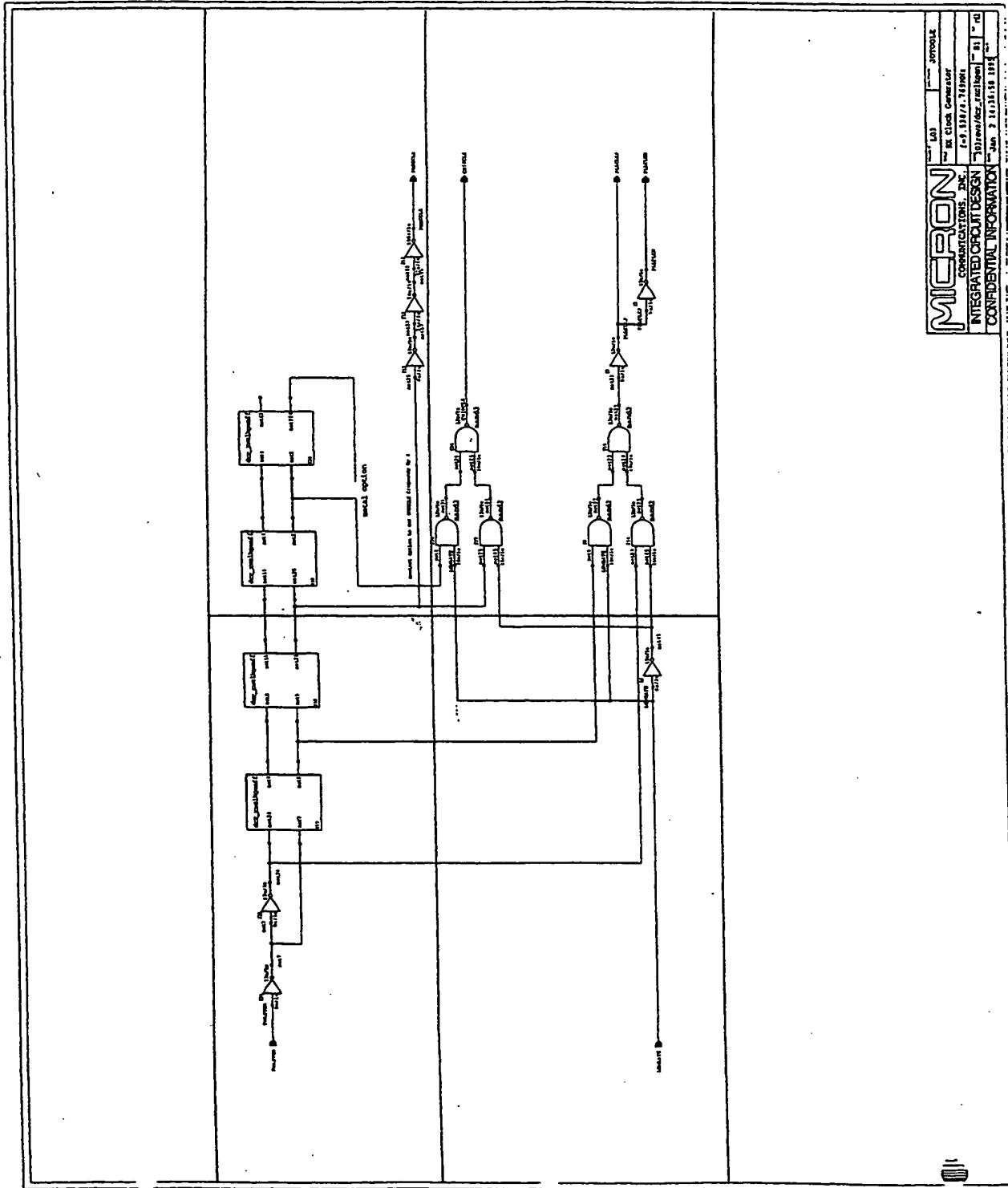
FIG. 8.0505

238, A

8.0506AA	8.0506AB
8.0506BA	8.0506BB

90508 6011

FIG. 8.0506



<b>MICRON</b>		LAJ	APPROVAL
COMMUNICATIONS, INC.		The Clock Generator	
INTEGRATED CIRCUIT DESIGN		1-9 3172.712001	
CONFIDENTIAL INFORMATION		Tolman/Dez, Inc./Jan 2 10:15:18 1973	



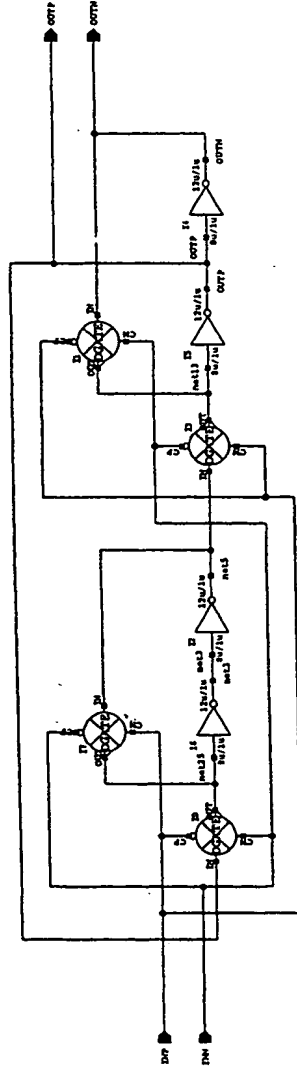


Fig. 8.050601

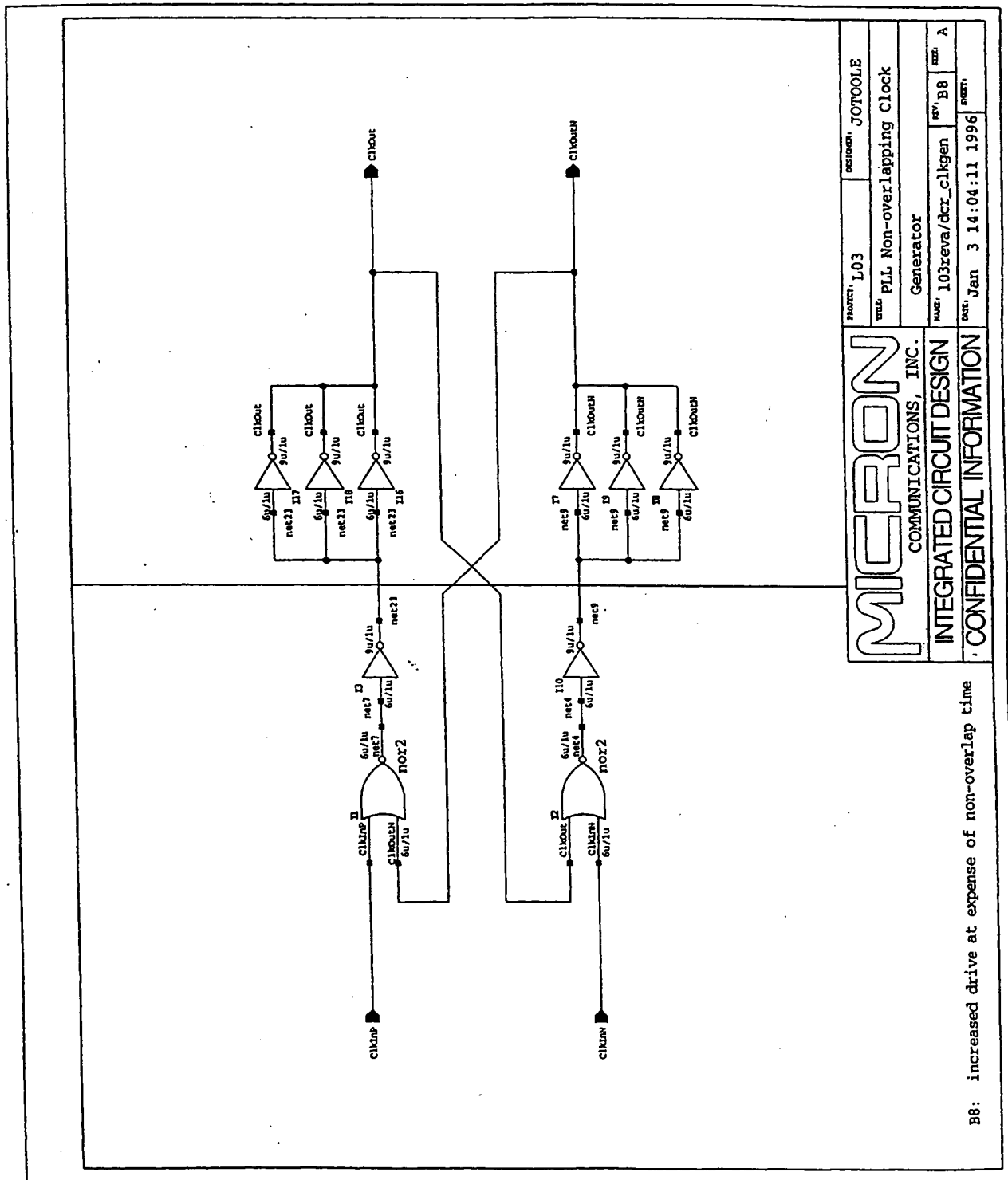
MICRON	PROPERTY: L03	REVISION: J0700LE
	NAME: Rx Clock Generator	
COMMUNICATIONS, INC.	Flip-Flop	
INTEGRATED CIRCUIT DESIGN	Thyrea/dcr_pxllegentf	Rev: B1
CONFIDENTIAL INFORMATION	Date: Sep 26 09:36:05 1994	

8.0507AB

8.0507AA

EEB.0507

Fig. 8.0507

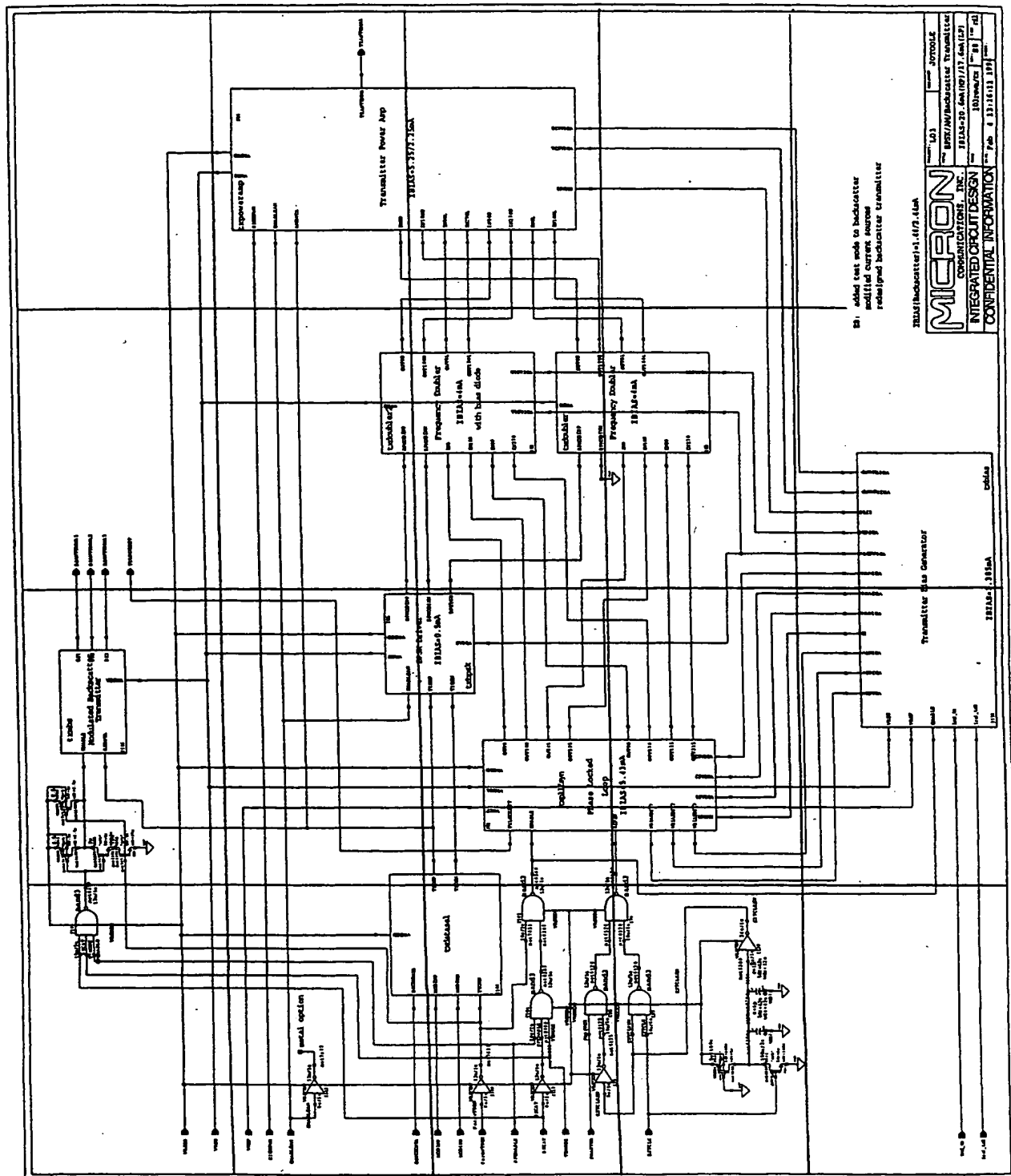


MICRON		PROPERTY: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: PLL Non-overlapping Clock	
INTEGRATED CIRCUIT DESIGN		Generator	
CONFIDENTIAL INFORMATION		NAME: 103reva/dcr_clkgen	REV: B8
		DATE: Jan 3 14:04:11 1996	DESIGN: A

B8: increased drive at expense of non-overlap time

8.06AA	8.06AB	8.06AC	8.06AD
8.06BA	8.06BB	8.06BC	8.06BD
8.06CA	8.06CB	8.06CC	8.06CD
8.06DA	8.06DB	8.06DC	8.06DD
8.06EA	8.06EB	8.06EC	8.06ED

IL 11 07 88.0016



51: added test mode to backdoor  
modified current source  
reassigned backdoor transmitter

TRANS (backdoor) v1.41/2.41/3.41/4.41

MICRON	
COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN	
CONFIDENTIAL INFORMATION	
Part #	13116113 1311
Rev	1
Date	10/17/87
By	10/17/87
Check	10/17/87
Appr	10/17/87
Drawn	10/17/87
Asm	10/17/87
Test	10/17/87
Ship	10/17/87
Store	10/17/87
Retire	10/17/87
Destroy	10/17/87

FIG. 8.06

8.0601AA	8.0601AB
8.0601BA	8.0601BB

EX 8.0601

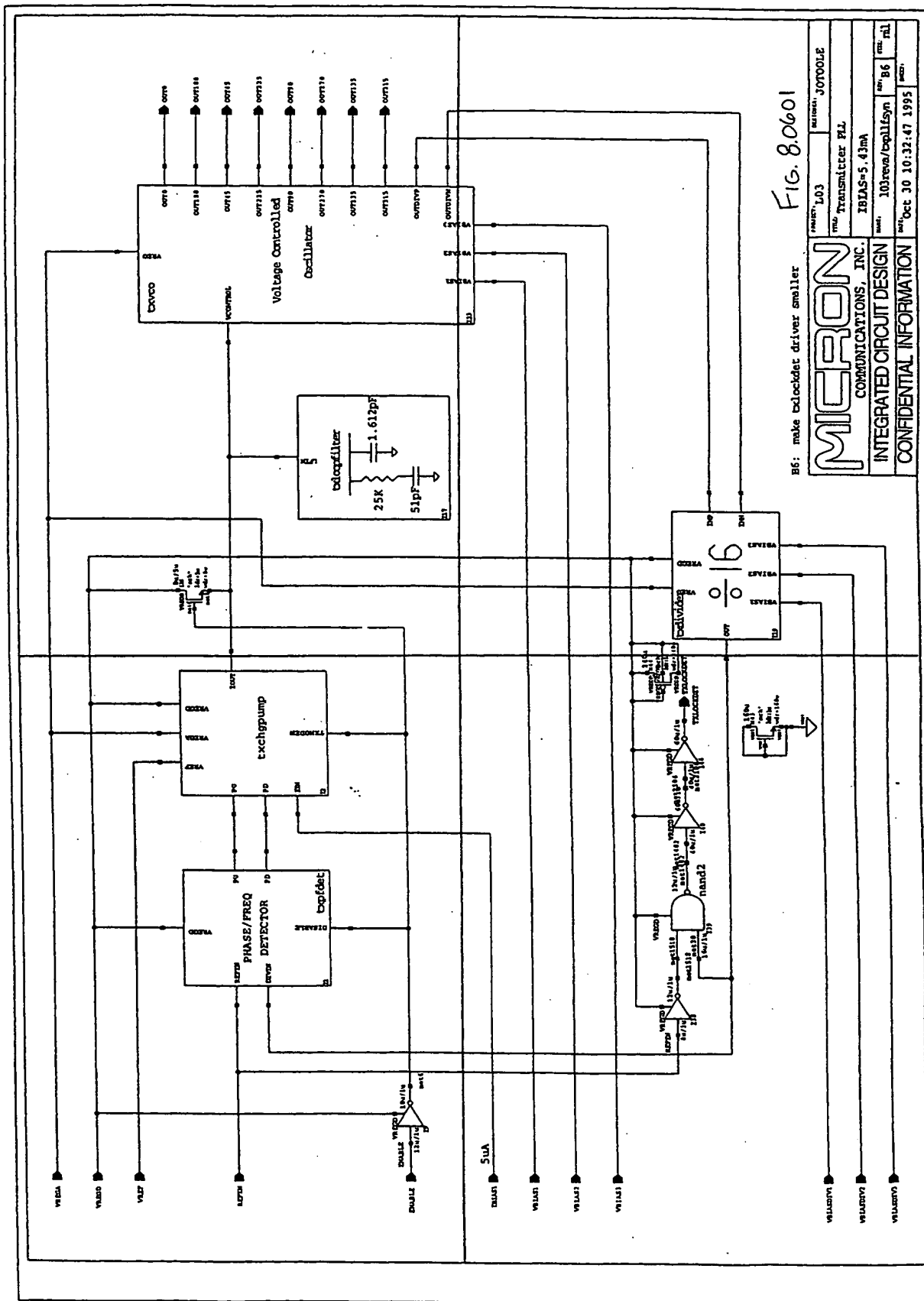


FIG. 8.0601

B5: make txclockdat driver smaller

MICRON		PROPERTY	LO3	REVISION	J07000LE
COMMUNICATIONS, INC.		TYPE	Transmitter PLL		
INTEGRATED CIRCUIT DESIGN		IBIAS	5.43mA		
CONFIDENTIAL INFORMATION		DATE	Oct 30 10:32:47 1995	REV	B6
		DESIGNER	nll		

8.060101AA	8.060101AB	8.060101AC
8.060101BA	8.060101BB	8.060101BC
8.060101CA	8.060101CB	8.060101CC

EX-8 B.060101



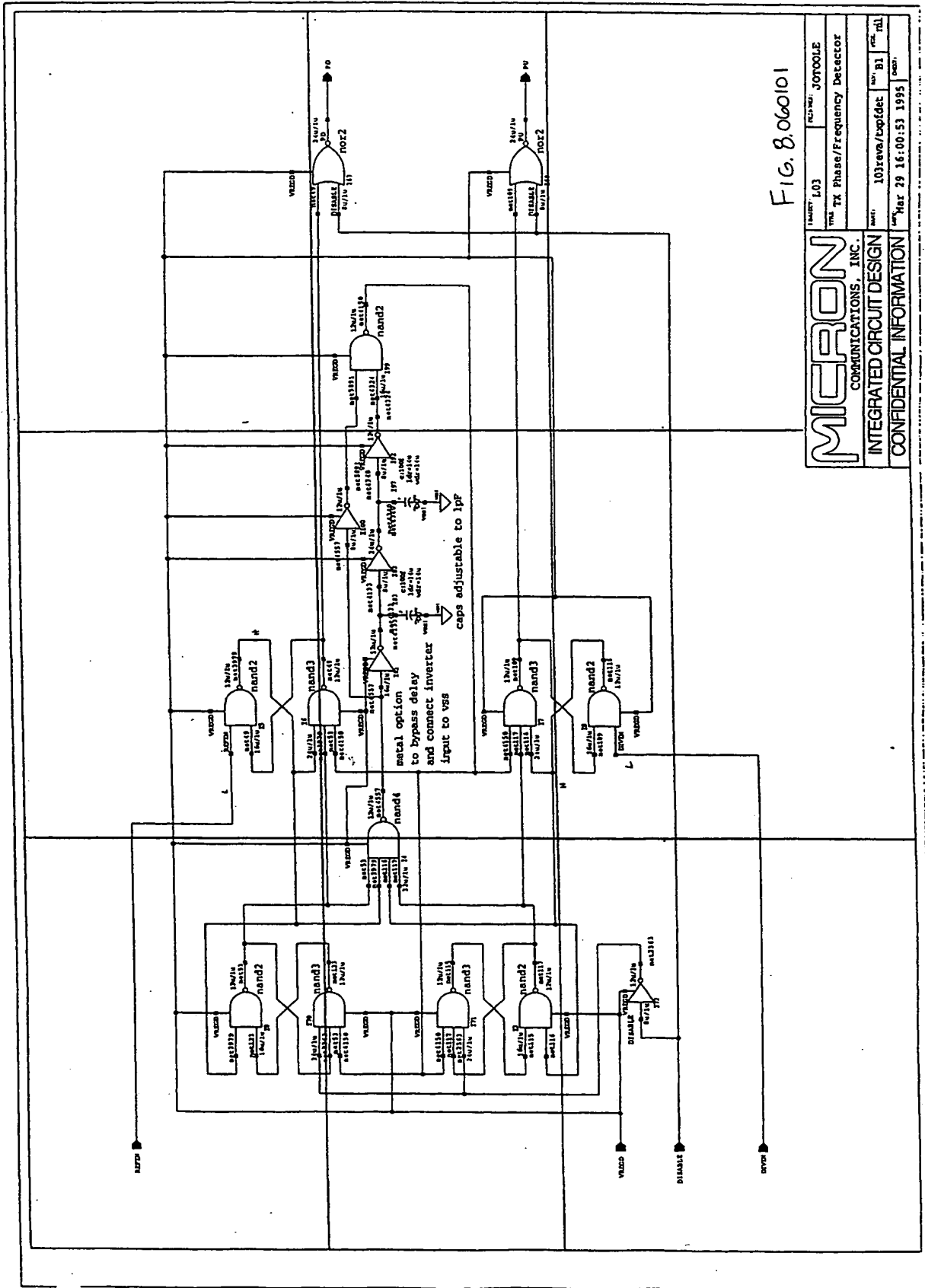


FIG. 8.060101

MICRON		REV. L03	REV. J07001E
COMMUNICATIONS, INC.		TX Phase/Frequency Detector	
INTEGRATED CIRCUIT DESIGN		REV. B1	REV. n11
CONFIDENTIAL INFORMATION		Mar 29 16:00:53 1995	

8.060102AA	8.060102AB
8.060102BA	8.060102BB

И. П. Б. 1902

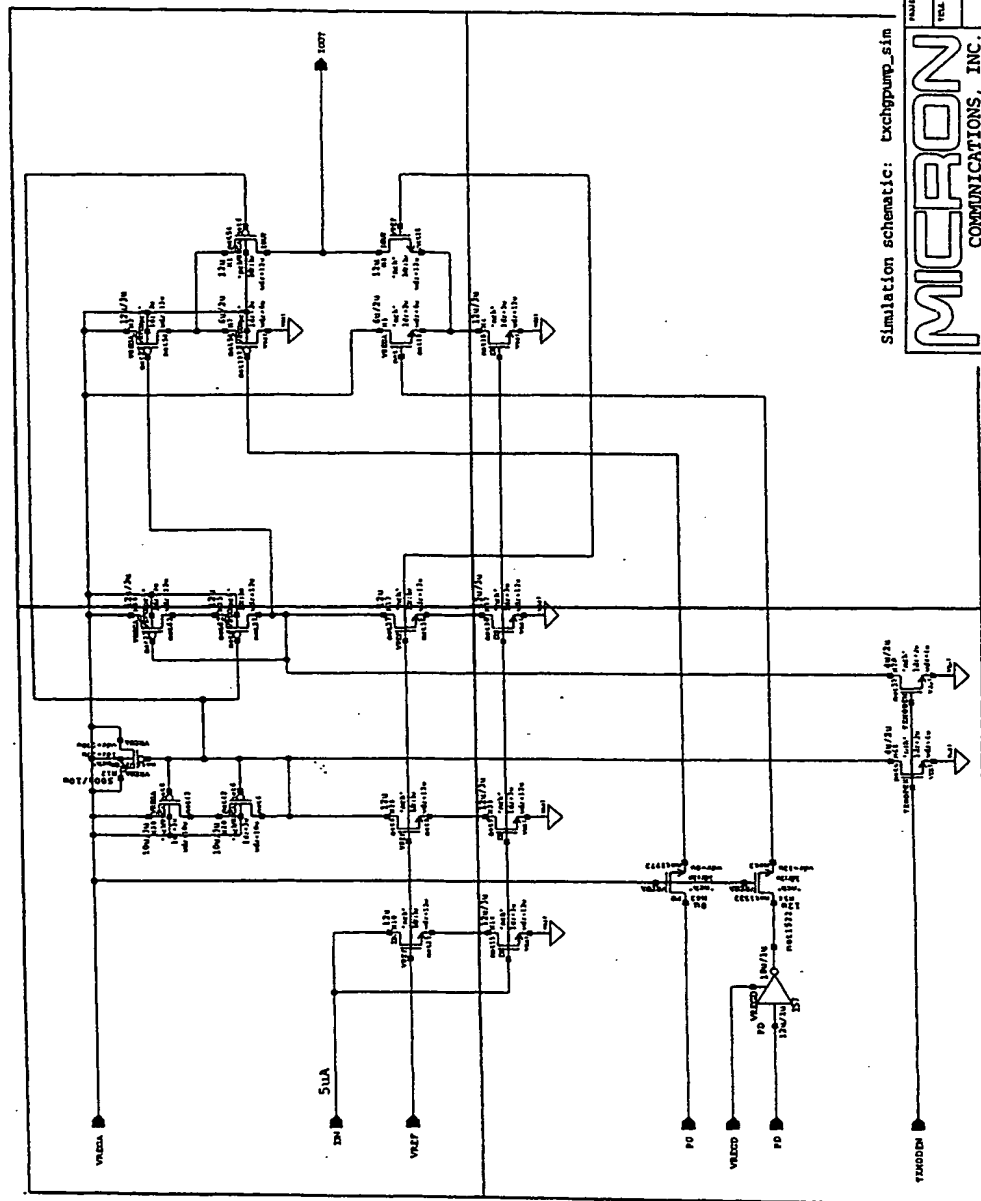


FIG. 8060102

Simulation schematic: txchgump\_sim

**MICRON**  
COMMUNICATIONS, INC.

PROJECT: 103	DESIGNER: JOTOOLE
FILE: TX PLL Charge Pump	
DATE: 103revA/txchgump	REV: B1
DATE: Feb 28 09:55:50 1995	REV: B1

INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

8.060103AA	8.060103AB
8.060103BA	8.060103BB
8.060103CA	8.060103CB

EEB.060103

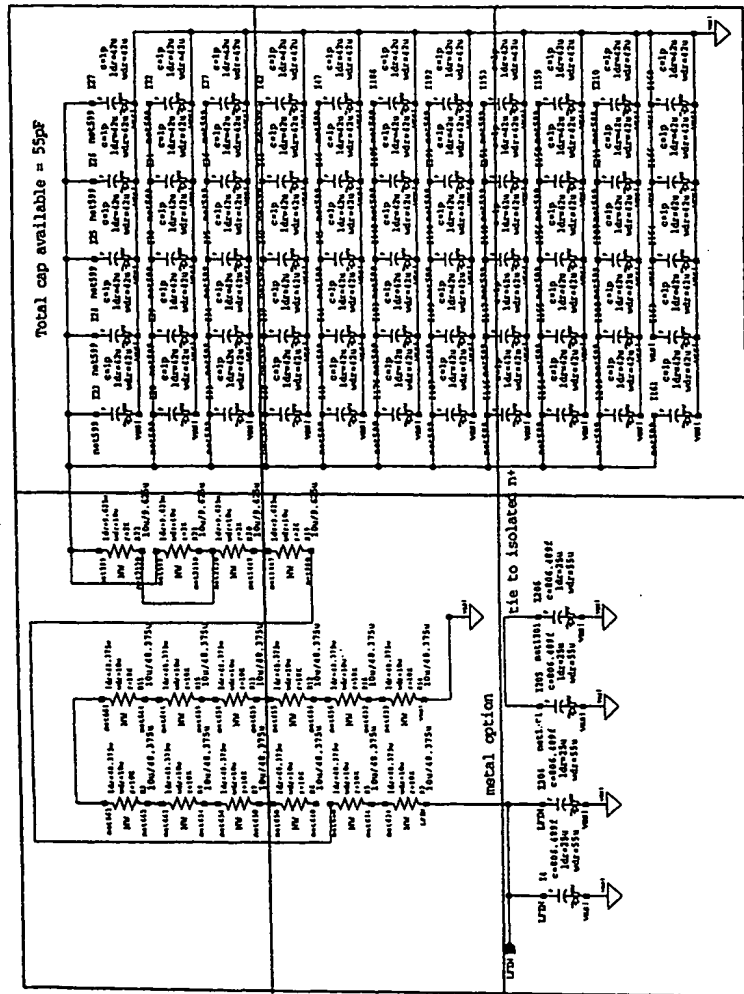


Fig. 8.060103

<b>MICRON</b>		PROJECT: L03	REVISION: J07001E
COMMUNICATIONS, INC.		TX PLL Loop Filter	
INTEGRATED CIRCUIT DESIGN		BW=700KHz	PH=60deg
CONFIDENTIAL INFORMATION		REV: B8	DATE: 5 14:40:11 1996

B2: moved extra caps to biasok  
B8: moved 2 2K resistors to lombs

8.060104AA	8.060104AB	8.060104AC
8.060104BA	8.060104BB	8.060104BC
8.060104CA	8.060104CB	8.060104CC
8.060104DA	8.060104DB	8.060104DC

# THE



8.06010401AA	8.06010401AB	8.06010401AC	8.06010401AD
8.06010401BA	8.06010401BB	8.06010401BC	8.06010401BD

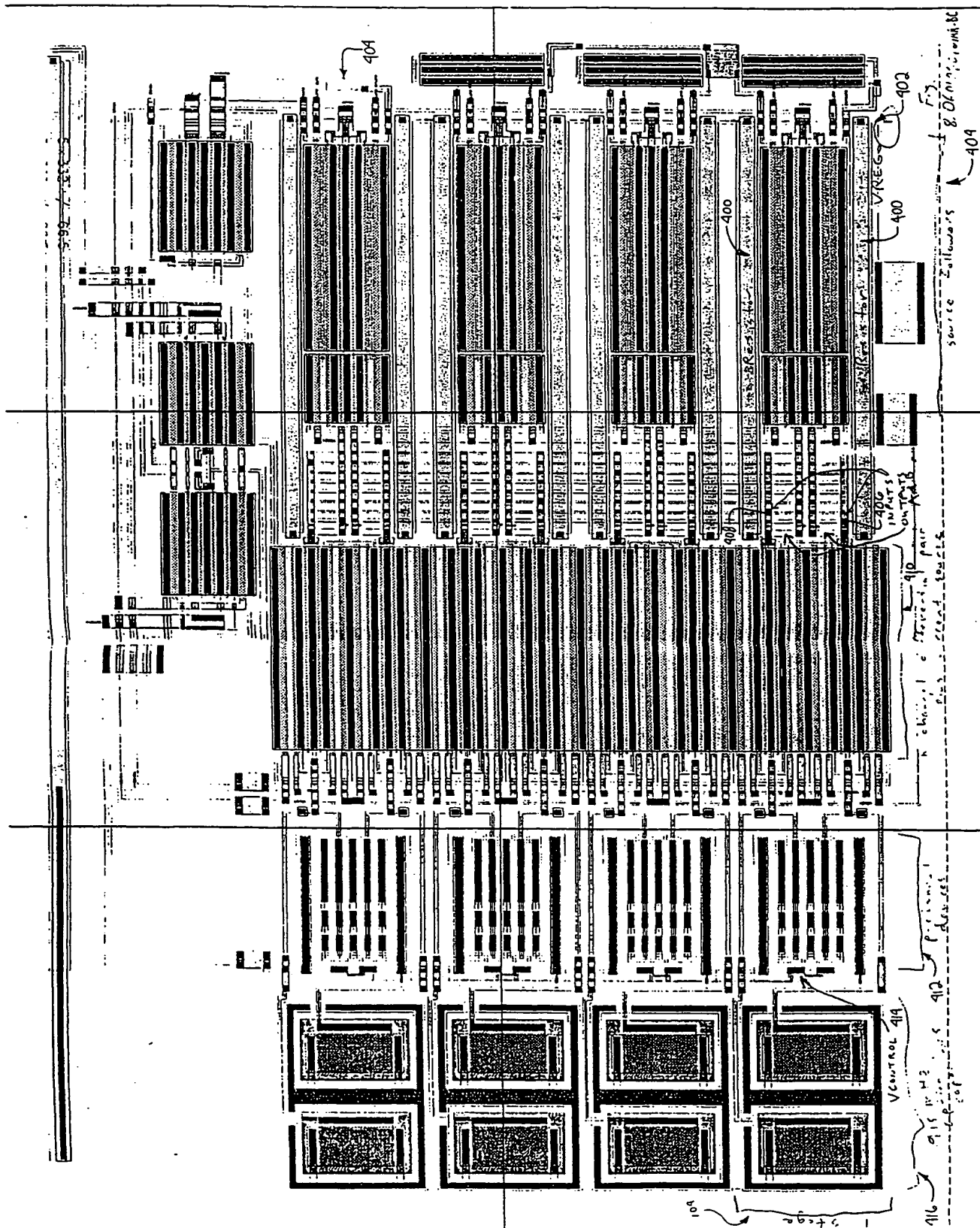
IL 507 88.06010401





8.0601040101AA	8.0601040101AB	8.0601040101AC
8.0601040101BA	8.0601040101BB	8.0601040101BC

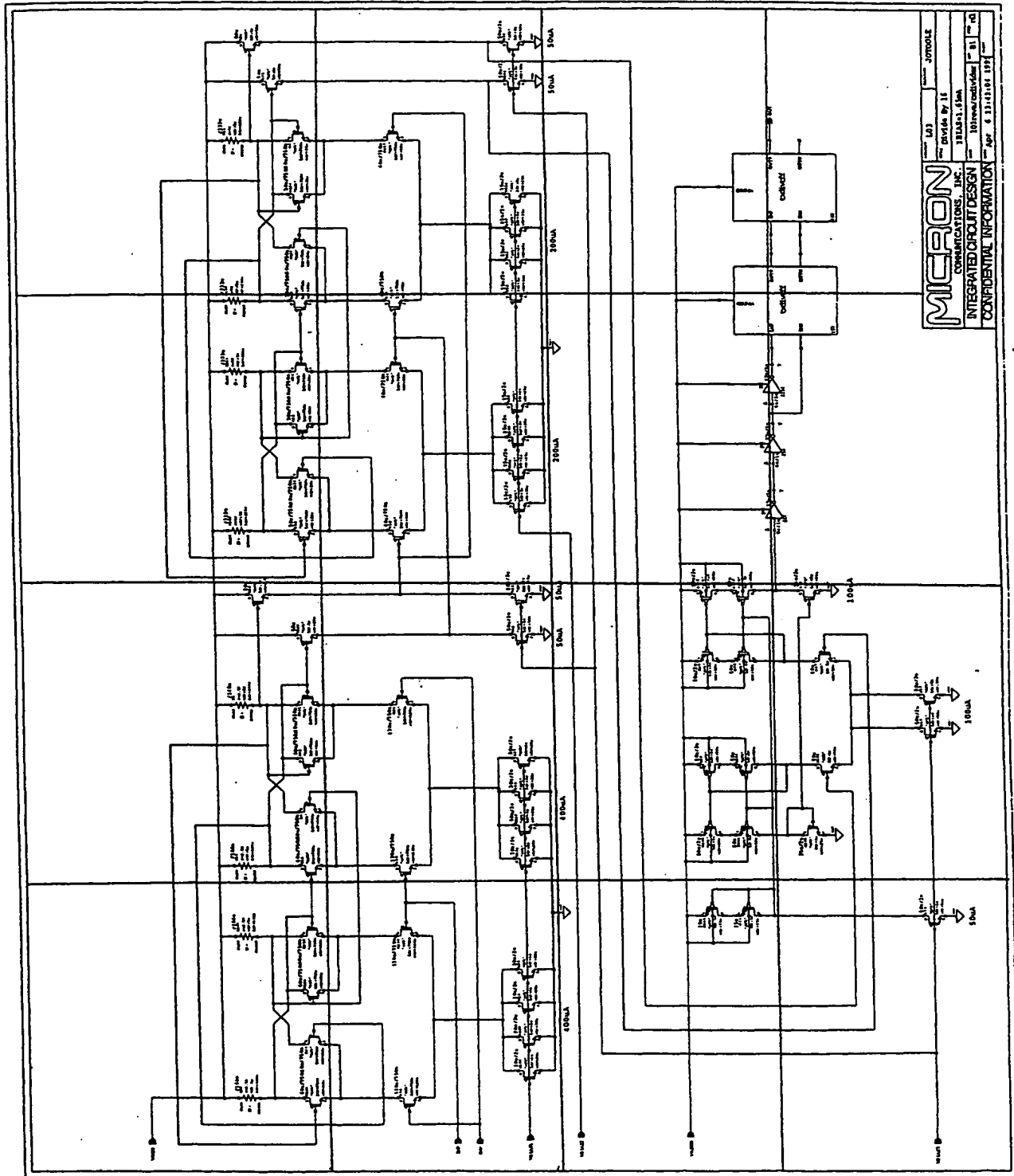
Итого: 8.060.100 руб.



8.060105AA	8.060105AB	8.060105AC	8.060105AD
8.060105BA	8.060105BB	8.060105BC	8.060105BD
8.060105CA	8.060105CB	8.060105CC	8.060105CD
8.060105DA	8.060105DB	8.060105DC	8.060105DD

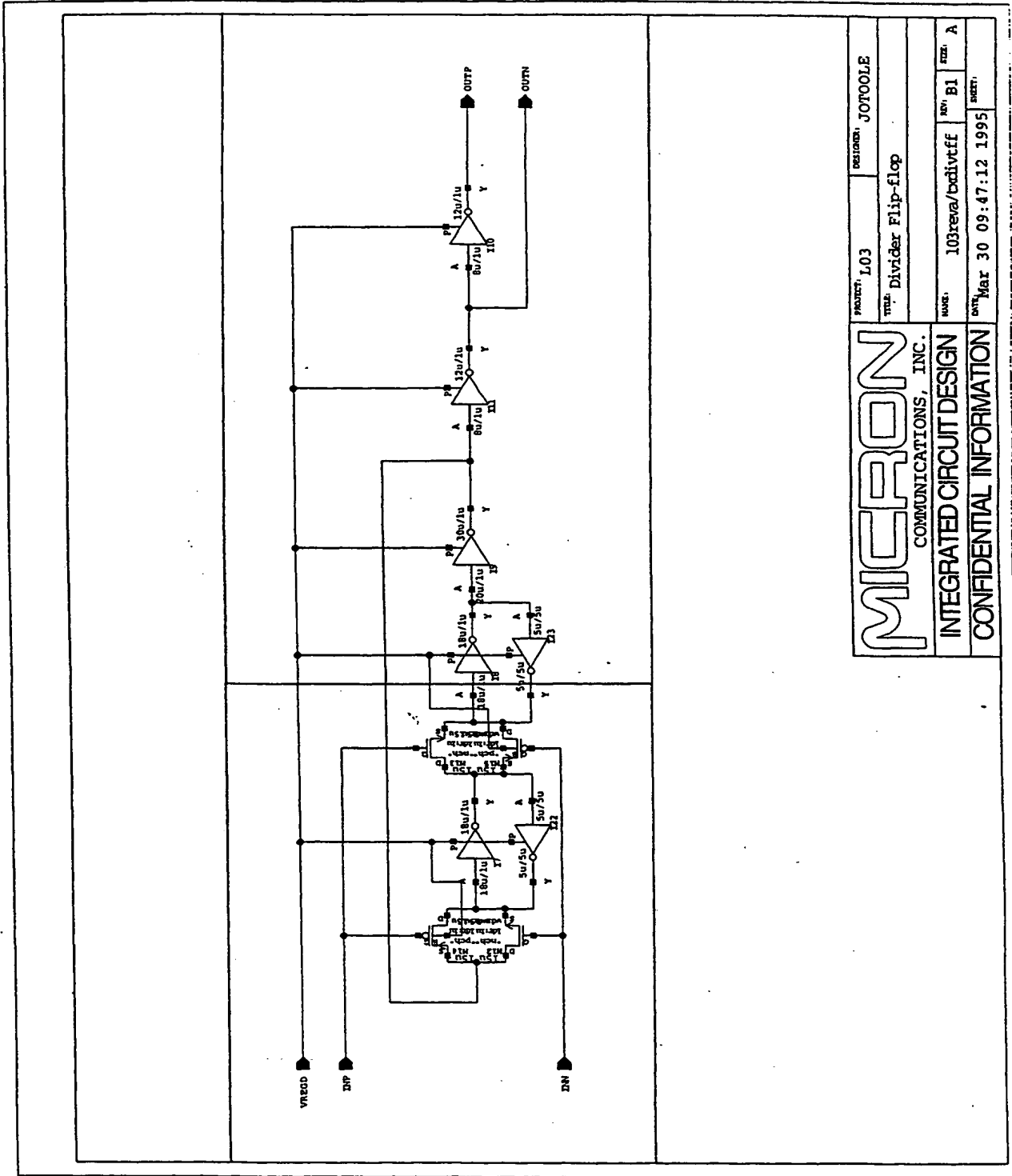
EX-88.060105

FIG. 8.060105



8.06010501AA	8.06010501AB
--------------	--------------

EX 8.06010501



MICRON		PROJECT: L03	DESIGNER: JOTFOOLE
COMMUNICATIONS, INC.		TITLE: Divider Flip-flop	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/bcdvtf	REV: B1
CONFIDENTIAL INFORMATION		DATE: Mar 30 09:47:12 1995	SHEET: A

FIG. 8.06010501

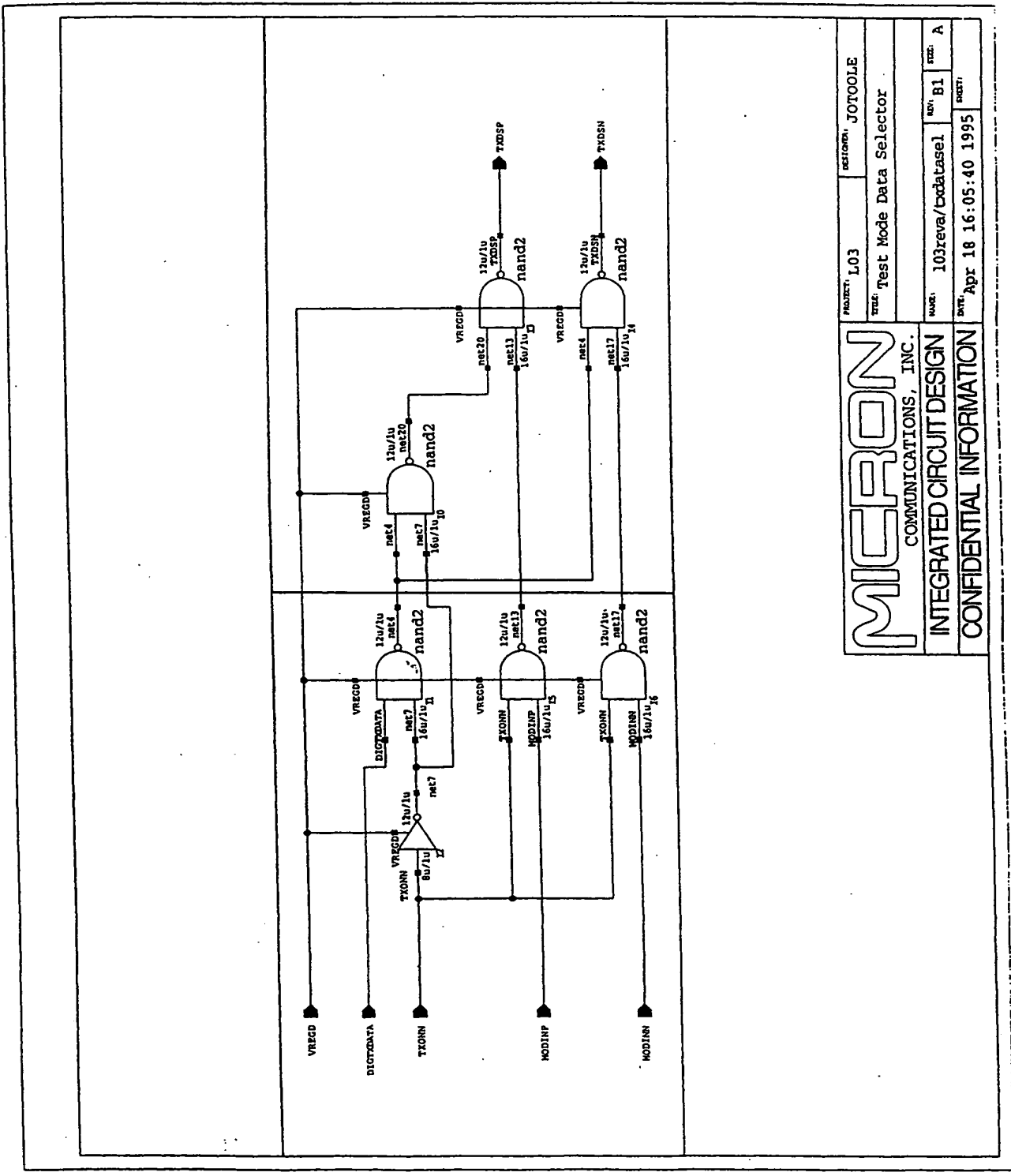
8.0602AA	8.0602AB
----------	----------

**8.0602AA**

Итого 8.050,2



FIG. 8.0602



MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Test Mode Data Selector	
INTEGRATED CIRCUIT DESIGN		WAVE: 103revb/bdatsel	REV: B1
CONFIDENTIAL INFORMATION		DATE: Apr 18 16:05:40 1995	FILE: A

8.0603AA	8.0603AB
----------	----------

EE 88.0603

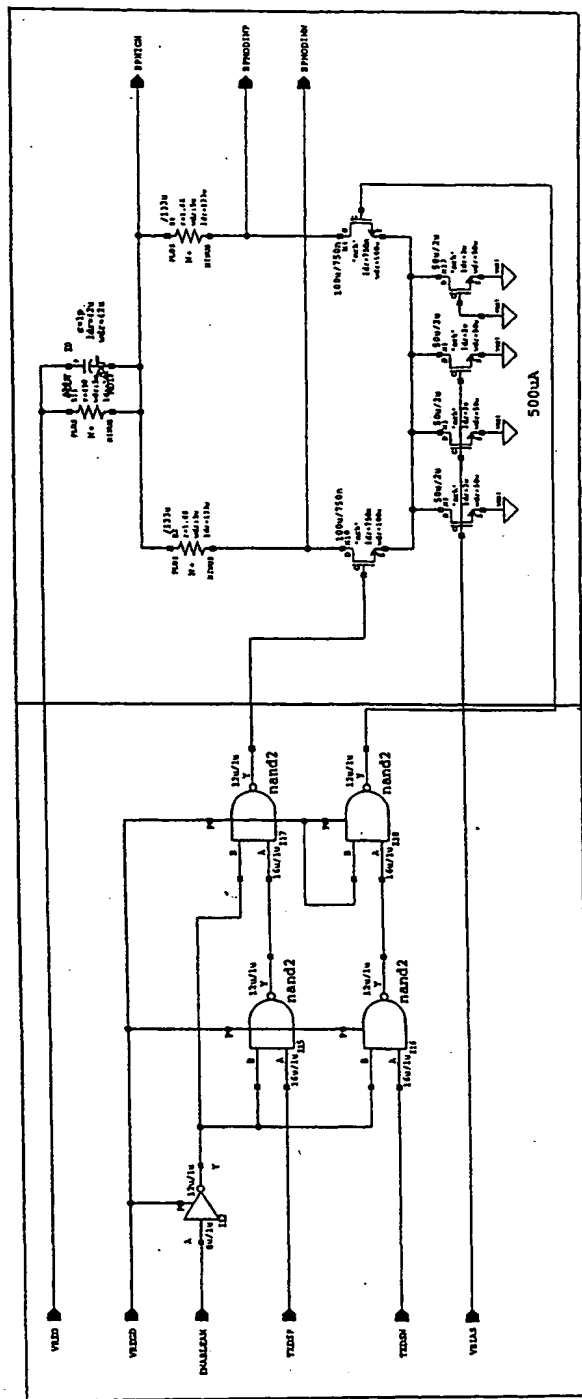


Fig. 8.0603

MICRON		PART: L03	REVISION: J0700LE
COMMUNICATIONS, INC.		TITLE: BPSK Modulation Driver	
INTEGRATED CIRCUIT DESIGN		IBIAS=500uA	
CONFIDENTIAL INFORMATION		DATE: 103revs/cdpsk	REV: B8
		JAN 18 10:28:46 1996	

B8: modified current source

8.0604AB

8.0604AA

8.0604AA

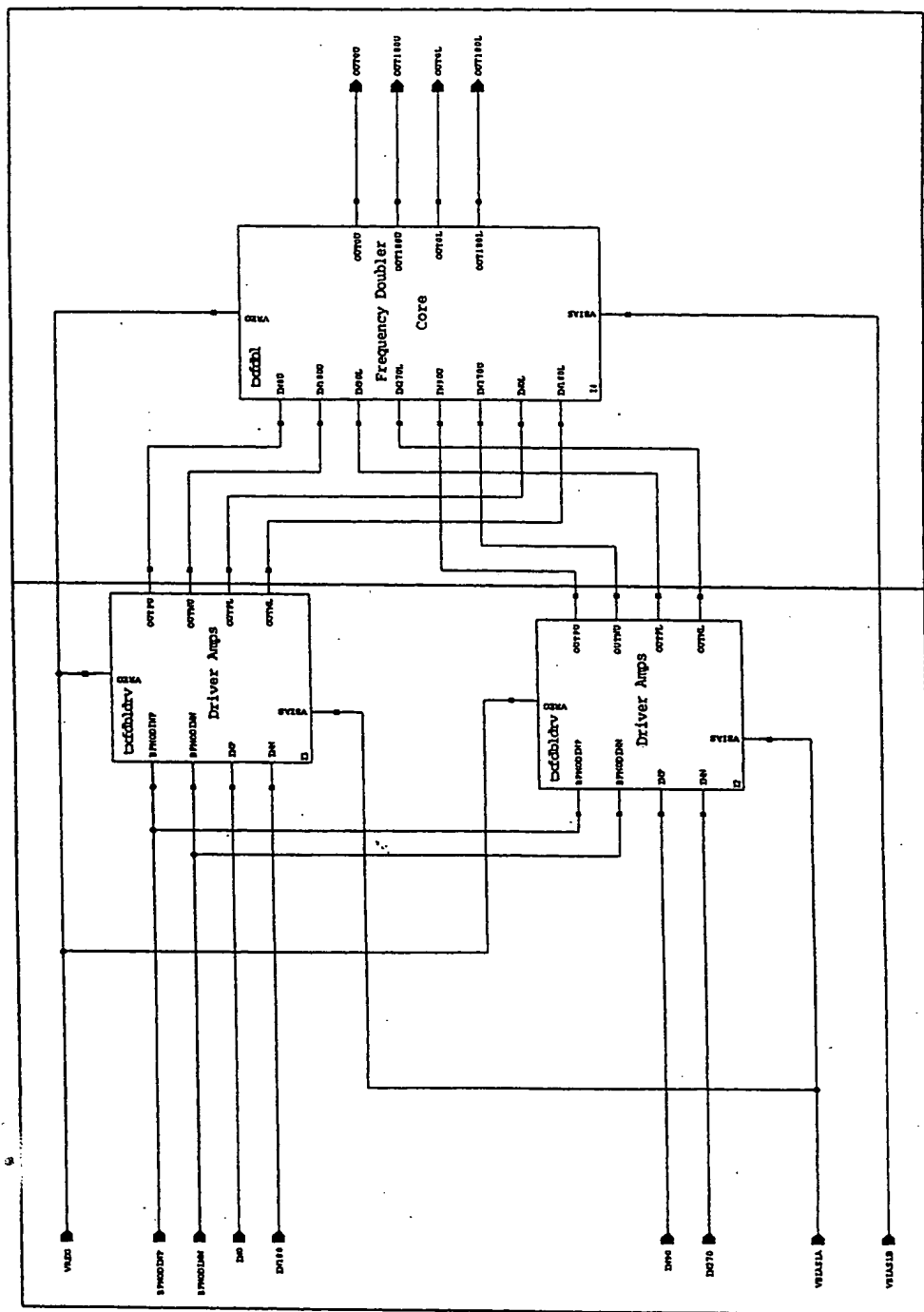
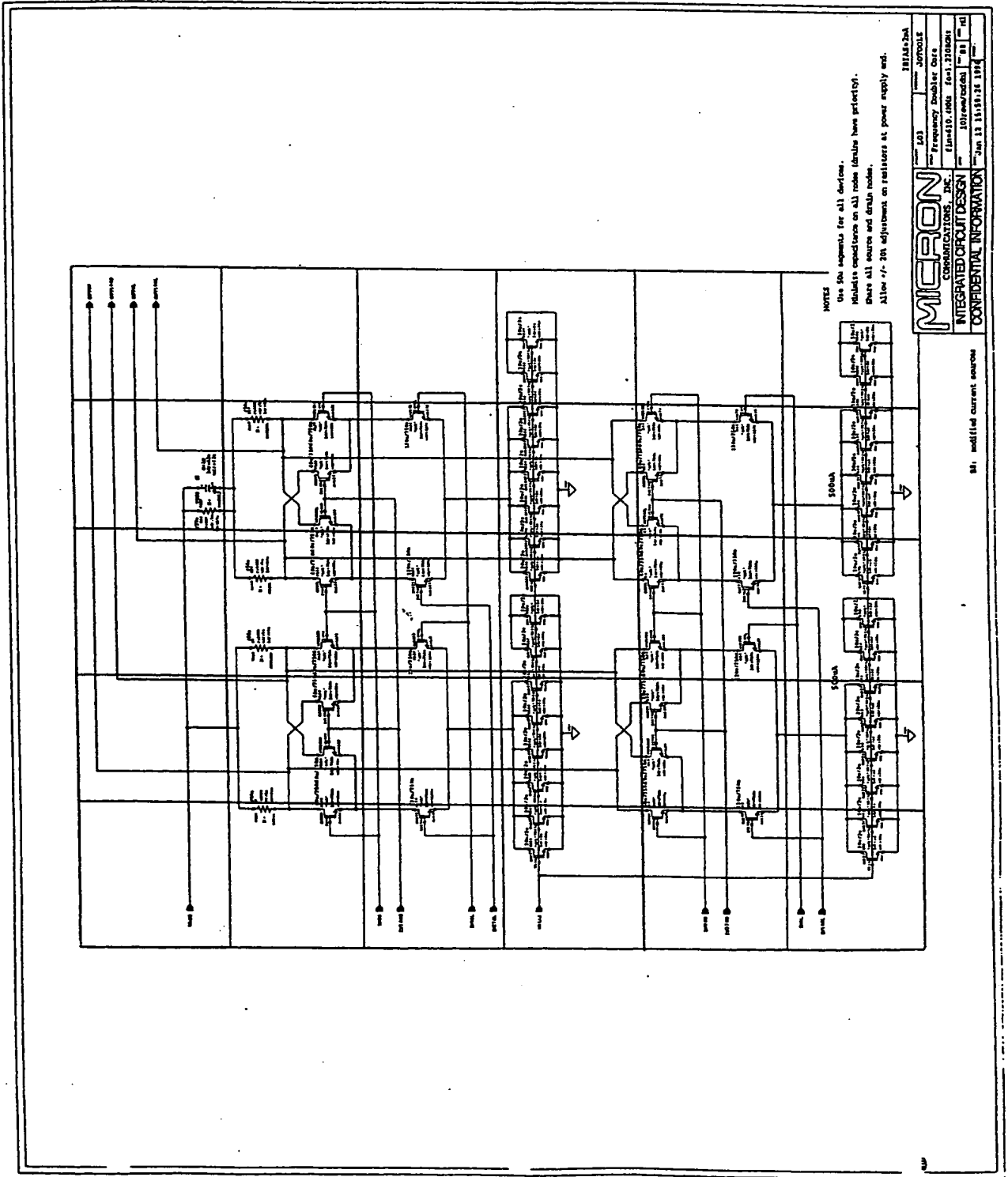


Fig. 8.0604

MICRON		PRODUCT: L03	REV: J0700LE
COMMUNICATIONS, INC.		Frequency Doubler	
INTEGRATED CIRCUIT DESIGN		IBTAS-4mA	
CONFIDENTIAL INFORMATION		DATE: 103revs/txdoubler	REV: B1
		DATE: Apr 5 10:17:13 1995	REV: 1110

8.060401AA	8.060401AB	8.060401AC	8.060401AD	8.060401AE
8.060401BA	8.060401BB	8.060401BC	8.060401BD	8.060401BE
8.060401CA	8.060401CB	8.060401CC	8.060401CD	8.060401CE
8.060401DA	8.060401DB	8.060401DC	8.060401DD	8.060401DE
8.060401EA	8.060401EB	8.060401EC	8.060401ED	8.060401EE
8.060401FA	8.060401FB	8.060401FC	8.060401FD	8.060401FE

II 8.060401



NOTES

Use 50k ohms for all devices.

Indicate capacitors on all nodes (value has priority).

Share all source and drain nodes.

Allow +/- 20% adjustment on resistors at power supply end.

101	101
102	102
103	103
104	104
105	105
106	106
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198	198
199	199
200	200

81: modified current sources

**MICRON**

COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN

CONFIDENTIAL INFORMATION

Jan 12 11:51:24 1994

Fig. 8.06.0901

8.0605AB

8.0605AA

8.0605



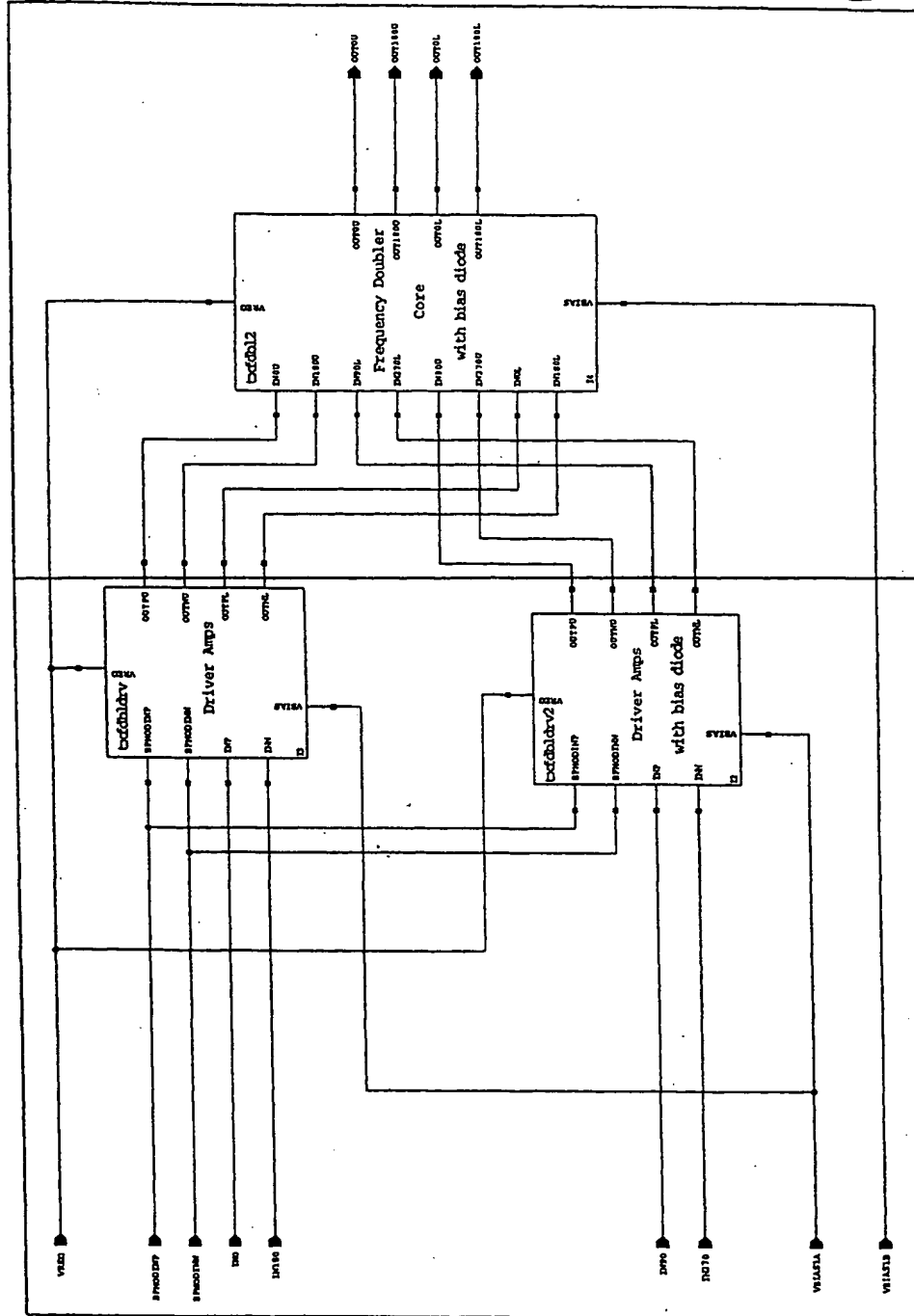


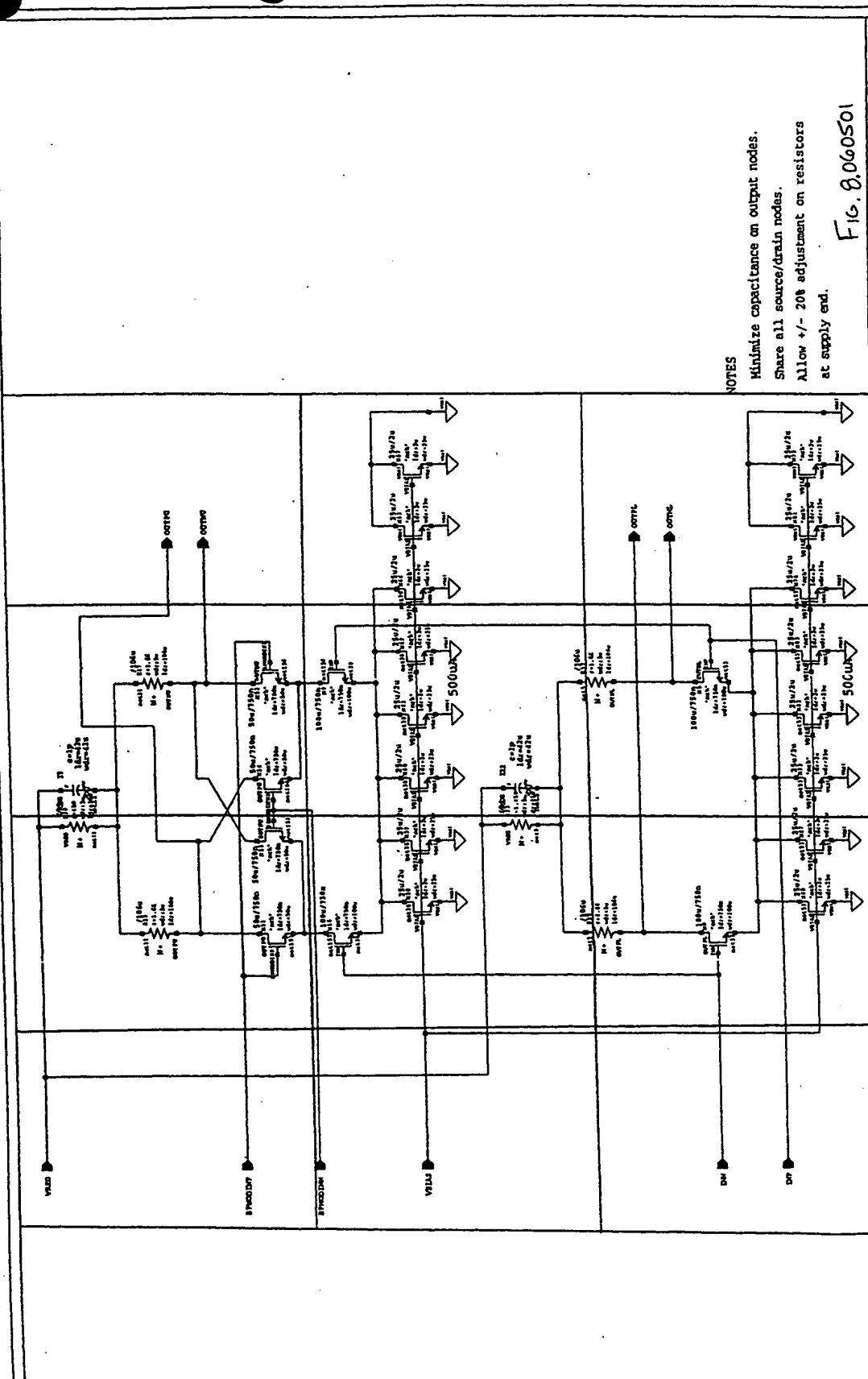
FIG. 8.0605

<b>MICRON</b>		REV. 1.03	DATE: 10/10/95	DESIGNER: JOTCOLE
COMMUNICATIONS, INC.		Frequency Doubler		
INTEGRATED CIRCUIT DESIGN		IBIAS=fma	REV. B8	FILE: fdl
CONFIDENTIAL INFORMATION		DATE: 10/10/95	DATE: 10/10/95	DATE: 10/10/95
		Jan 12 17:22:51 1996		

B8: current sources modified

<i>8.060501AA</i>	<i>8.060501AB</i>	<i>8.060501AC</i>	<i>8.060501AD</i>
<i>8.060501BA</i>	<i>8.060501BB</i>	<i>8.060501BC</i>	<i>8.060501BD</i>
<i>8.060501CA</i>	<i>8.060501CB</i>	<i>8.060501CC</i>	<i>8.060501CD</i>

IEG *8.060501*



NOTES

- Minimize capacitance on output nodes.
- Share all source/drain nodes.
- Allow +/- 20% adjustment on resistors at supply end.

FIG. 8.060501

MICRON		DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		DATE: 103
INTEGRATED CIRCUIT DESIGN		PROJECT: Doubler Driver Amps
CONFIDENTIAL INFORMATION		IBIAS-10A
		REV: 103rev/bcd/bldv
		REV: 88
		DATE: Jan 12 15:37:26 1996

B8: modified current sources

8.060502AA	8.060502AB	8.060502AC	8.060502AD
8.060502BA	8.060502BB	8.060502BC	8.060502BD
8.060502CA	8.060502CB	8.060502CC	8.060502CD

Fig 8.060502



8.060503AA	8.060503AB	8.060503AC	8.060503AD	8.060503AE
8.060503BA	8.060503BB	8.060503BC	8.060503BD	8.060503BE
8.060503CA	8.060503CB	8.060503CC	8.060503CD	8.060503CE
8.060503DA	8.060503DB	8.060503DC	8.060503DD	8.060503DE
8.060503EA	8.060503EB	8.060503EC	8.060503ED	8.060503EE
8.060503FA	8.060503FB	8.060503FC	8.060503FD	8.060503FE

И И 8.060503

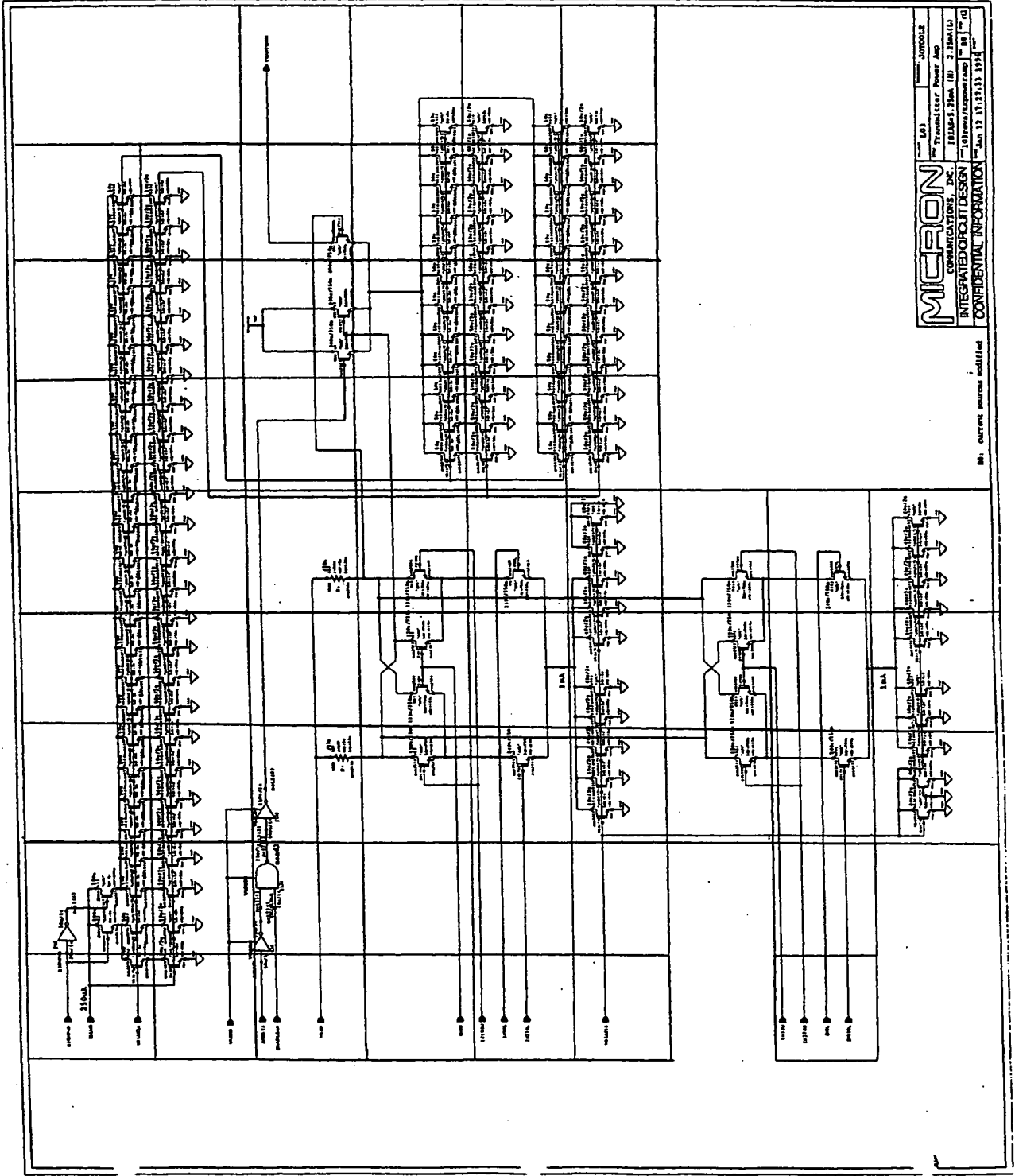


8.0606AA	8.0606AB	8.0606AC	8.0606AD	8.0606AE	8.0606AF	8.0606AG	8.0606AH
8.0606BA	8.0606BB	8.0606BC	8.0606BD	8.0606BE	8.0606BF	8.0606BG	8.0606BH
8.0606CA	8.0606CB	8.0606CC	8.0606CD	8.0606CE	8.0606CF	8.0606CG	8.0606CH
8.0606DA	8.0606DB	8.0606DC	8.0606DD	8.0606DE	8.0606DF	8.0606DG	8.0606DH
8.0606EA	8.0606EB	8.0606EC	8.0606ED	8.0606EE	8.0606EF	8.0606EG	8.0606EH
8.0606FA	8.0606FB	8.0606FC	8.0606FD	8.0606FE	8.0606FF	8.0606FG	8.0606FH
		8.0606GC	8.0606GD	8.0606GE			
8.0606HA	8.0606HB	8.0606HC	8.0606HD	8.0606HE			
	8.0606IB	8.0606IC	8.0606ID	8.0606IE			


 DEPARTMENT OF DEFENSE



FIG. 8.0606

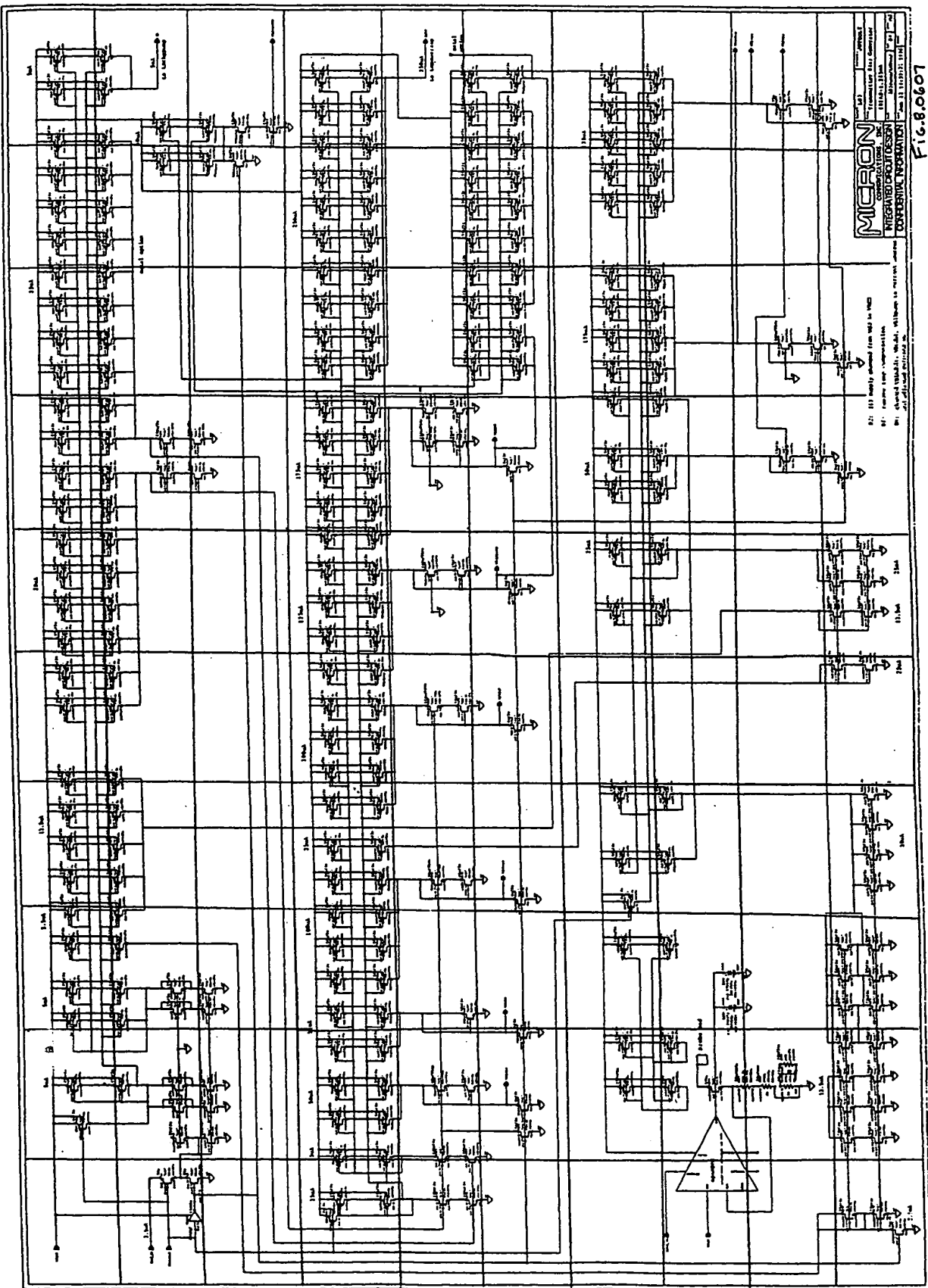


8.0607AA	8.0607AB	8.0607AC	8.0607AD	8.0607AE	8.0607AF	8.0607AG	8.0607AH	8.0607AI	8.0607AJ
8.0607BA	8.0607BB	8.0607BC	8.0607BD	8.0607BE	8.0607BF	8.0607BG	8.0607BH	8.0607BI	8.0607BJ
8.0607CA	8.0607CB	8.0607CC	8.0607CD	8.0607CE	8.0607CF	8.0607CG	8.0607CH	8.0607CI	8.0607CJ
8.0607DA	8.0607DB	8.0607DC	8.0607DD	8.0607DE	8.0607DF	8.0607DG	8.0607DH	8.0607DI	8.0607DJ
8.0607EA	8.0607EB	8.0607EC	8.0607ED	8.0607EE	8.0607EF	8.0607EG	8.0607EH	8.0607EI	8.0607EJ
8.0607FA	8.0607FB	8.0607FC	8.0607FD	8.0607FE	8.0607FF	8.0607FG	8.0607FH	8.0607FI	8.0607FJ
8.0607GA	8.0607GB	8.0607GC	8.0607GD	8.0607GE	8.0607GF	8.0607GG	8.0607GH	8.0607GI	8.0607GJ
8.0607HA	8.0607HB	8.0607HC	8.0607HD	8.0607HE	8.0607HF	8.0607HG	8.0607HH	8.0607HI	8.0607HJ
8.0607IA	8.0607IB	8.0607IC	8.0607ID	8.0607IE	8.0607IF	8.0607IG	8.0607IH	8.0607II	8.0607IJ
8.0607JA	8.0607JB	8.0607JC	8.0607JD	8.0607JE	8.0607JF	8.0607JG	8.0607JH	8.0607JI	8.0607JJ

К. П. 07 88.006007

Fig. 8.0607

**MicroN**  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION  
DATE 11/10/77  
REV. 1.0



1. 111 Input signal from 101 to 102  
2. 101 Input signal from 101 to 102  
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93. 101 Input signal from 101 to 102  
94. 101 Input signal from 101 to 102  
95. 101 Input signal from 101 to 102  
96. 101 Input signal from 101 to 102  
97. 101 Input signal from 101 to 102  
98. 101 Input signal from 101 to 102  
99. 101 Input signal from 101 to 102  
100. 101 Input signal from 101 to 102

8.0608AA	8.0608AB
8.0608BA	8.0608BB

II II BB.0150BB

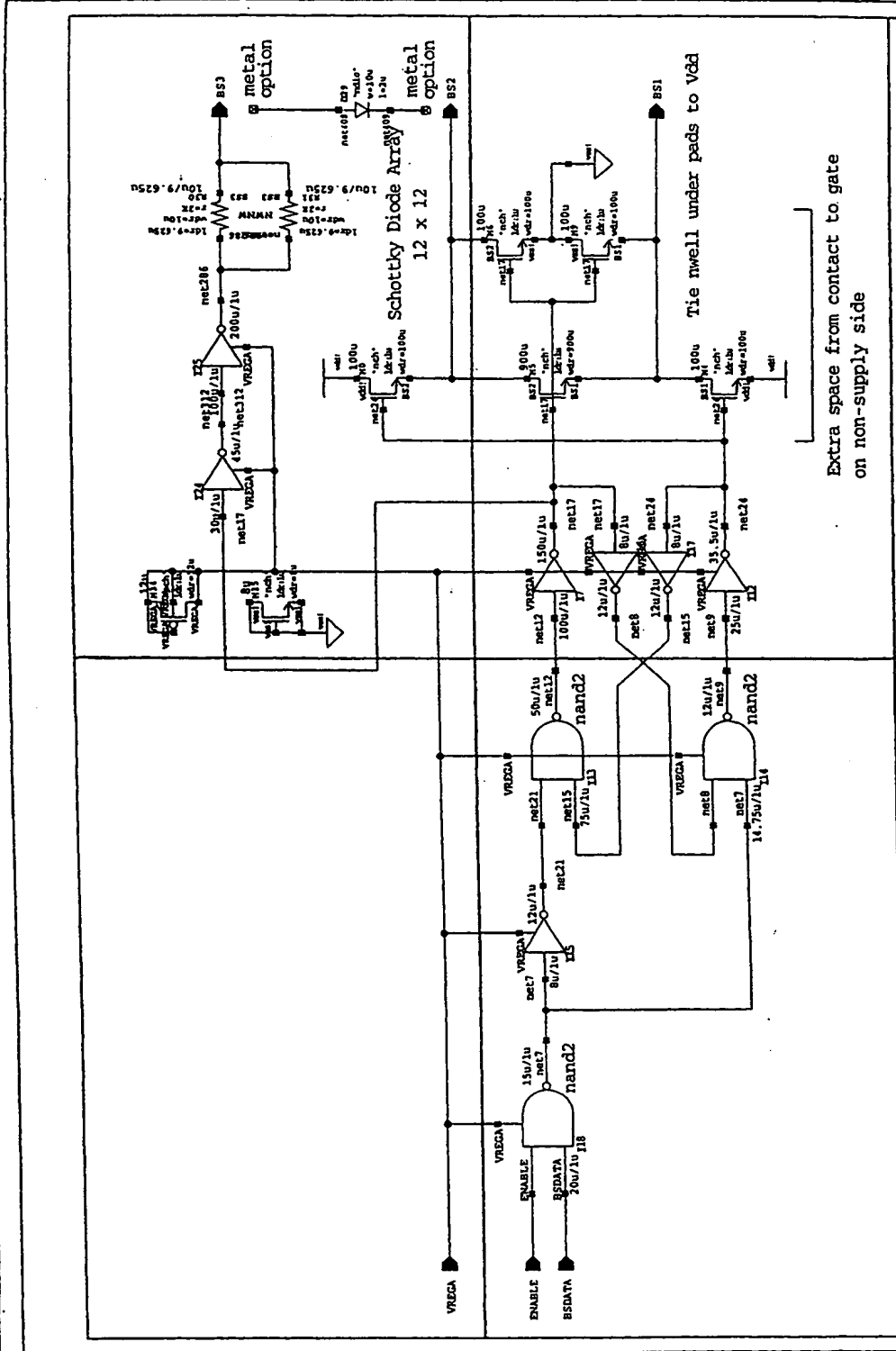


Fig. 8.0608

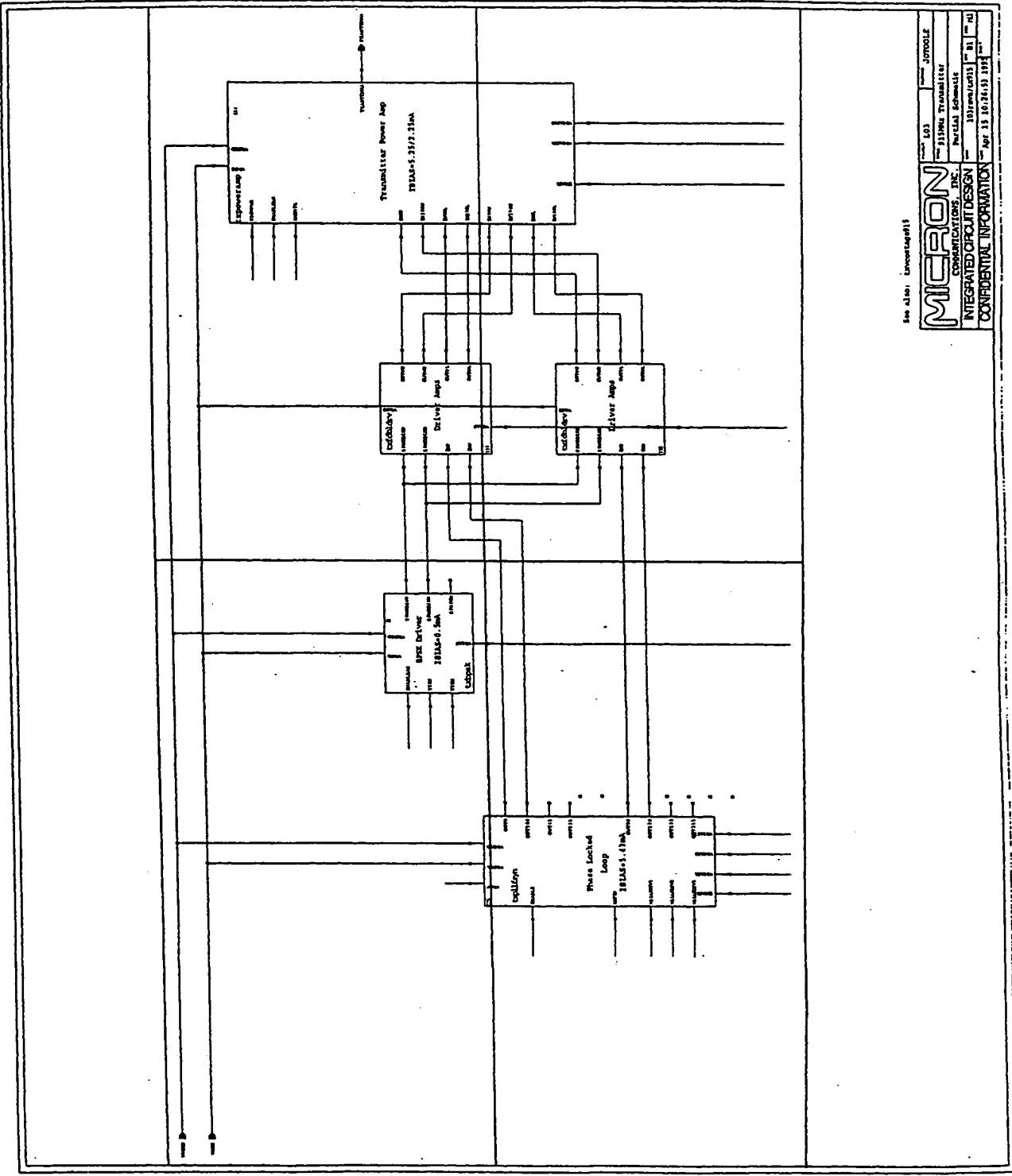
MICRON		PROJECT: L03	DESIGNED: JOTOOLE
COMMUNICATIONS, INC.		NAME: Modulated Backscatter	
INTEGRATED CIRCUIT DESIGN		TRANSMITTER	
CONFIDENTIAL INFORMATION		NAME: 103reva/ombs	REV: B10
		DATE: Mar 26 11:07:42 1996	SIZE: A

B8: initial release of this design  
B10: disconnected inverter

8.07AB	8.07BB
8.07AA	8.07BA

BB.007L

Fig. 8.07



See also: Unpublished

<b>MICRON</b>		Part No.	103	Rev.	000001
MICRON COMMUNICATIONS, INC.		Product	315MHz Transmitter	Part No.	103
INTEGRATED CIRCUIT DESIGN		Product	Partial Schematic	Part No.	103
CONFIDENTIAL INFORMATION		Date	Apr 15 1978	Page	1

8.0701AA	8.0701AB
8.0701BA	8.0701BB
8.0701CA	8.0701CB

EE 88.0701

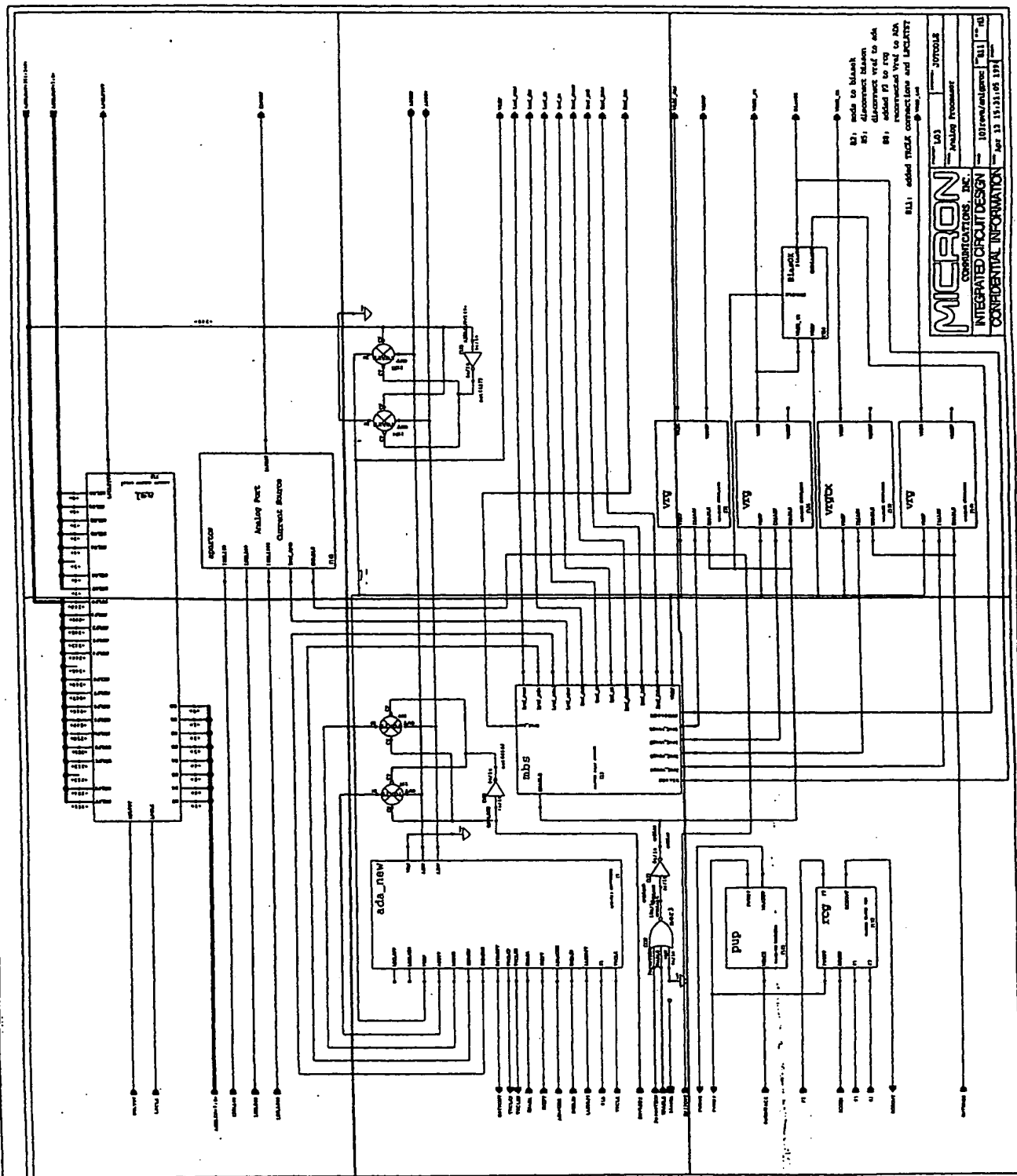




9AA	9AB
9BA	9BB
9CA	9CB

SECRET

Fig. 9



9.01AA	9.01AB	9.01AC	9.01AD	9.01AE	9.01AF	9.01AG	9.01AH
9.01BA	9.01BB	9.01BC	9.01BD	9.01BE	9.01BF	9.01BG	9.01BH
9.01CA	9.01CB	9.01CC	9.01CD	9.01CE	9.01CF	9.01CG	9.01CH
9.01DA	9.01DB	9.01DC	9.01DD	9.01DE	9.01DF	9.01DG	9.01DH

II II II II II

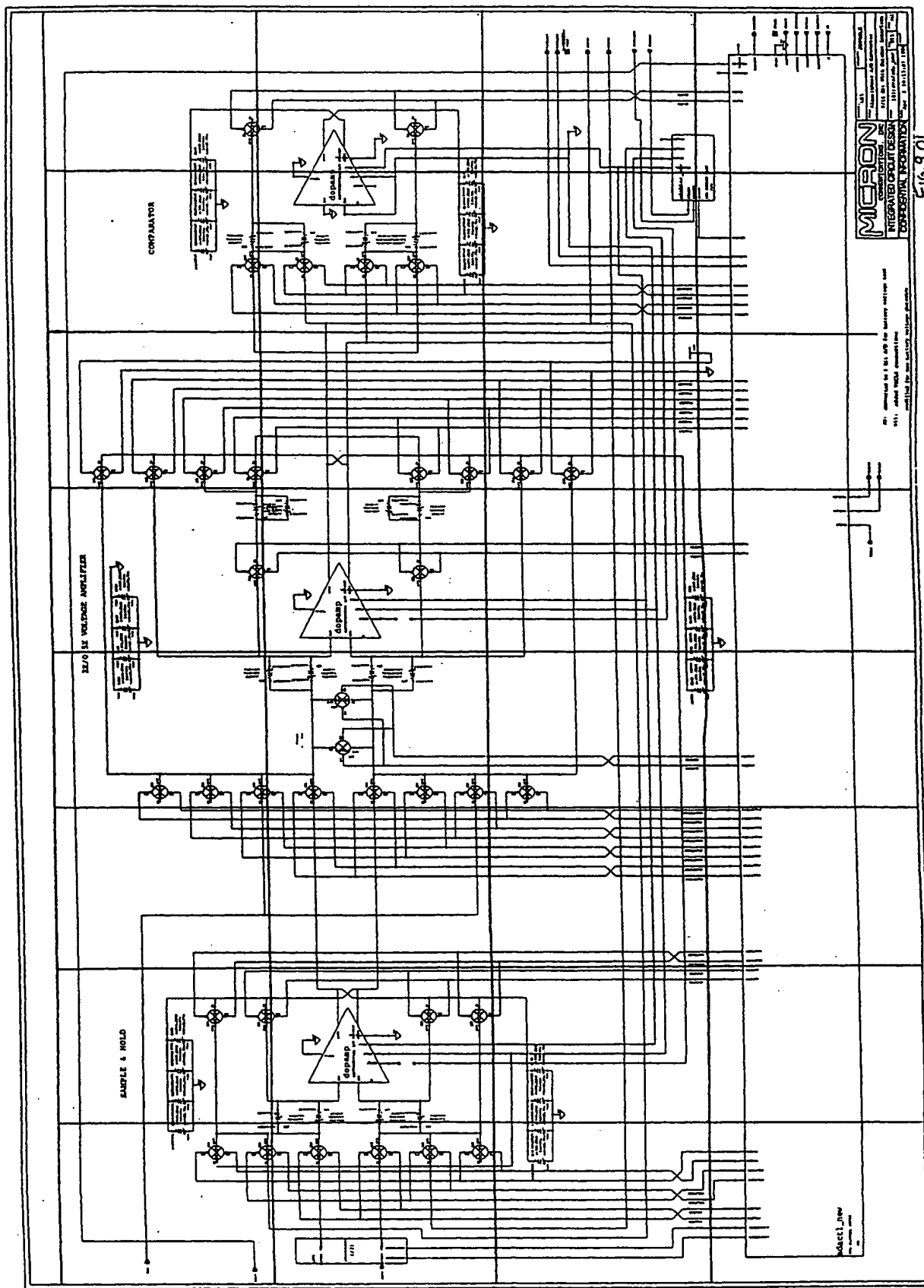
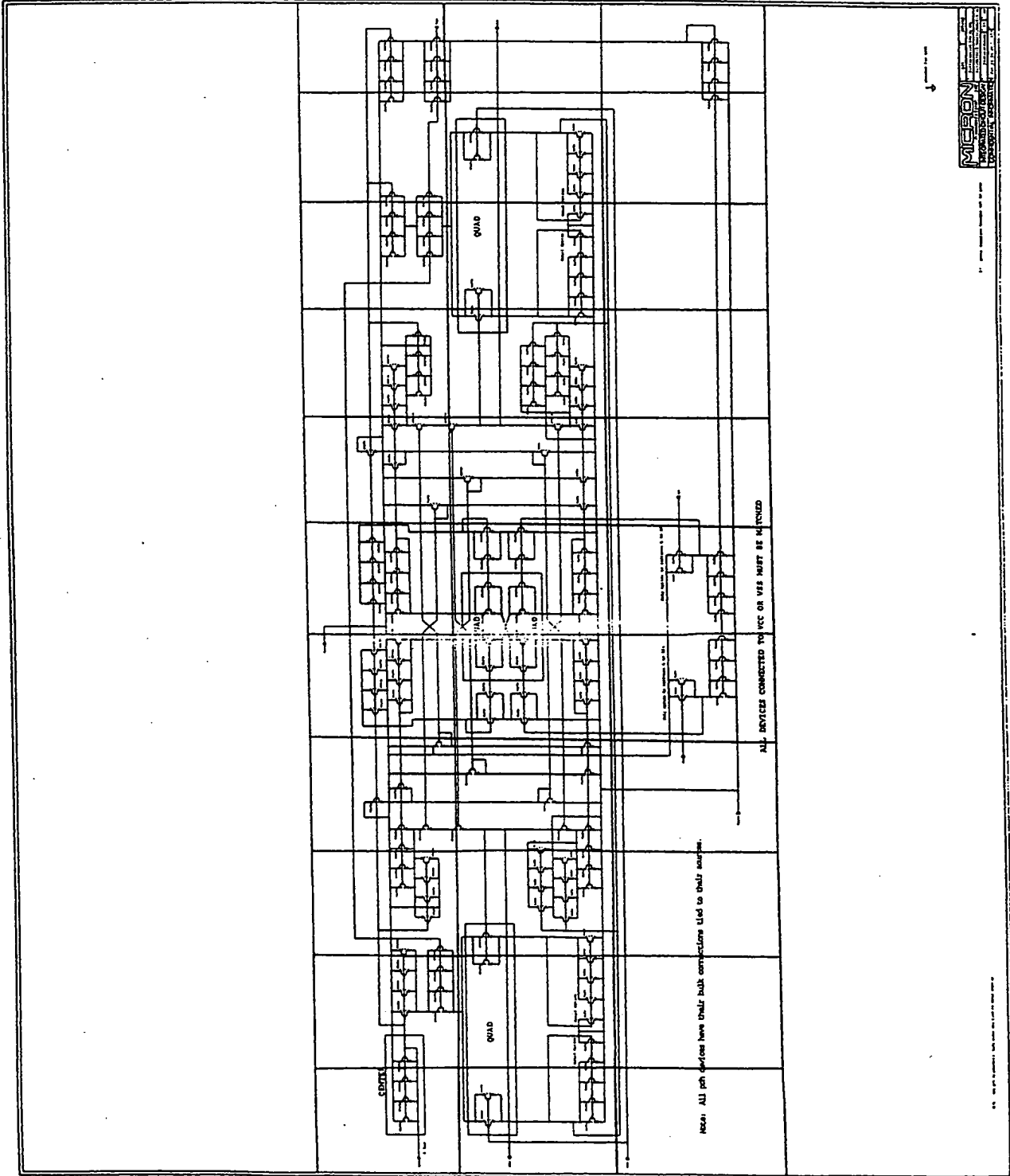


Fig. 9.01

9.0101AA	9.0101AB	9.0101AC	9.0101AD	9.0101AE	9.0101AF	9.0101AG	9.0101AH	9.0101AI	9.0101AJ	9.0101AK
9.0101BA	9.0101BB	9.0101BC	9.0101BD	9.0101BE	9.0101BF	9.0101BG	9.0101BH	9.0101BI	9.0101BJ	9.0101BK
9.0101CA	9.0101CB	9.0101CC	9.0101CD	9.0101CE	9.0101CF	9.0101CG	9.0101CH	9.0101CI	9.0101CJ	9.0101CK

II 9.0101

FIG. 9.0101

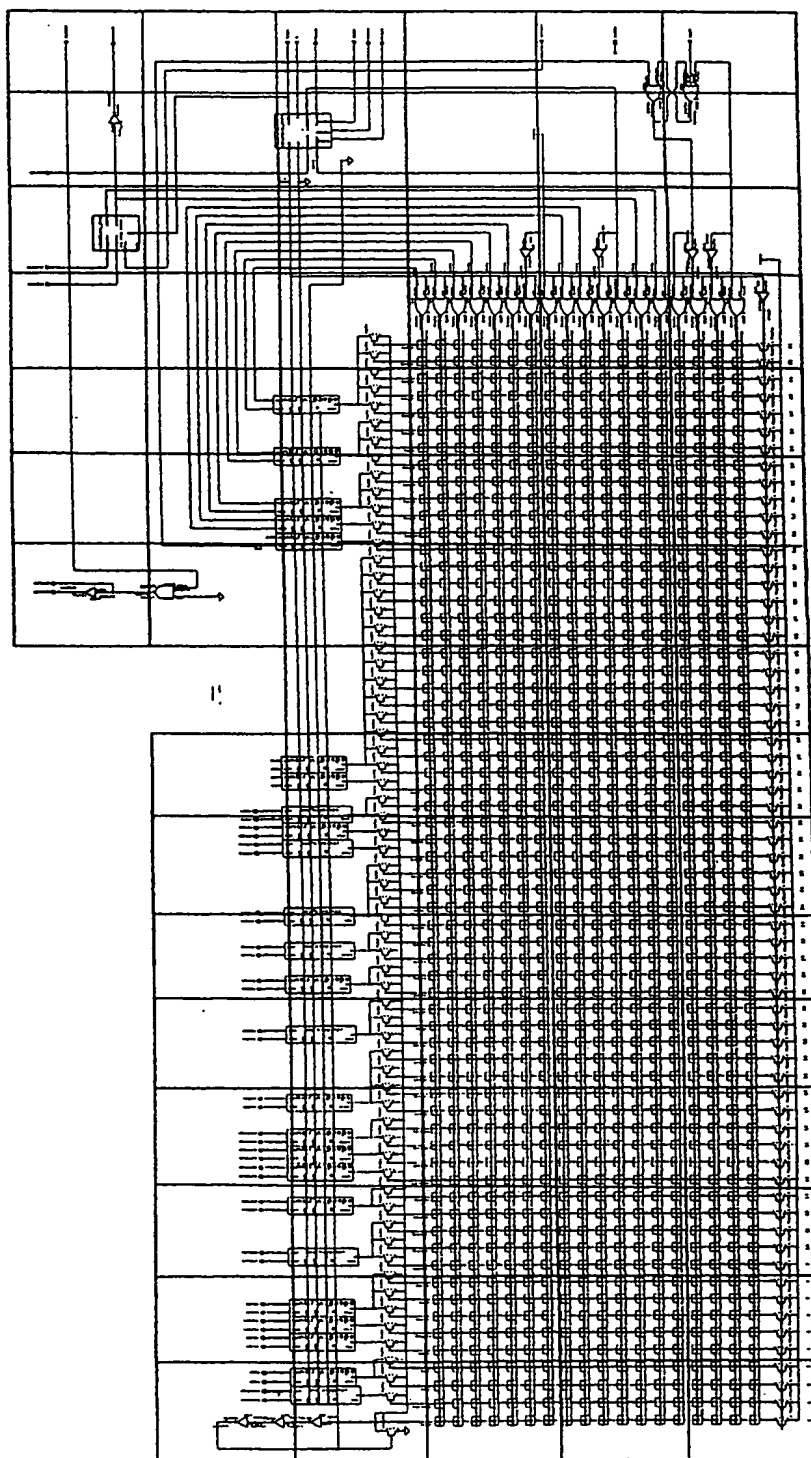






9.0103BA	9.0103BB	9.0103BC	9.0103BD	9.0103BE	9.0103BF	9.0103BG	9.0103BH		9.0103AJ	9.0103AK	9.0103AL	9.0103AM	9.0103AN	9.0103AO	9.0103AP
9.0103CA	9.0103CB	9.0103CC	9.0103CD	9.0103CE	9.0103CF	9.0103CG	9.0103CH	9.0103CI	9.0103BJ	9.0103BK	9.0103BL	9.0103BM	9.0103BN	9.0103BO	9.0103BP
9.0103DA	9.0103DB	9.0103DC	9.0103DD	9.0103DE	9.0103DF	9.0103DG	9.0103DH	9.0103DI	9.0103DJ	9.0103DK	9.0103DL	9.0103DM	9.0103DN	9.0103DO	9.0103DP
9.0103EA	9.0103EB	9.0103EC	9.0103ED	9.0103EE	9.0103EF	9.0103EG	9.0103EH	9.0103EI	9.0103EJ	9.0103EK	9.0103EL	9.0103EM	9.0103EN	9.0103EO	9.0103EP
9.0103FA	9.0103FB	9.0103FC	9.0103FD	9.0103FE	9.0103FF	9.0103FG	9.0103FH	9.0103FI	9.0103FJ	9.0103FK	9.0103FL	9.0103FM	9.0103FN	9.0103FO	9.0103FP

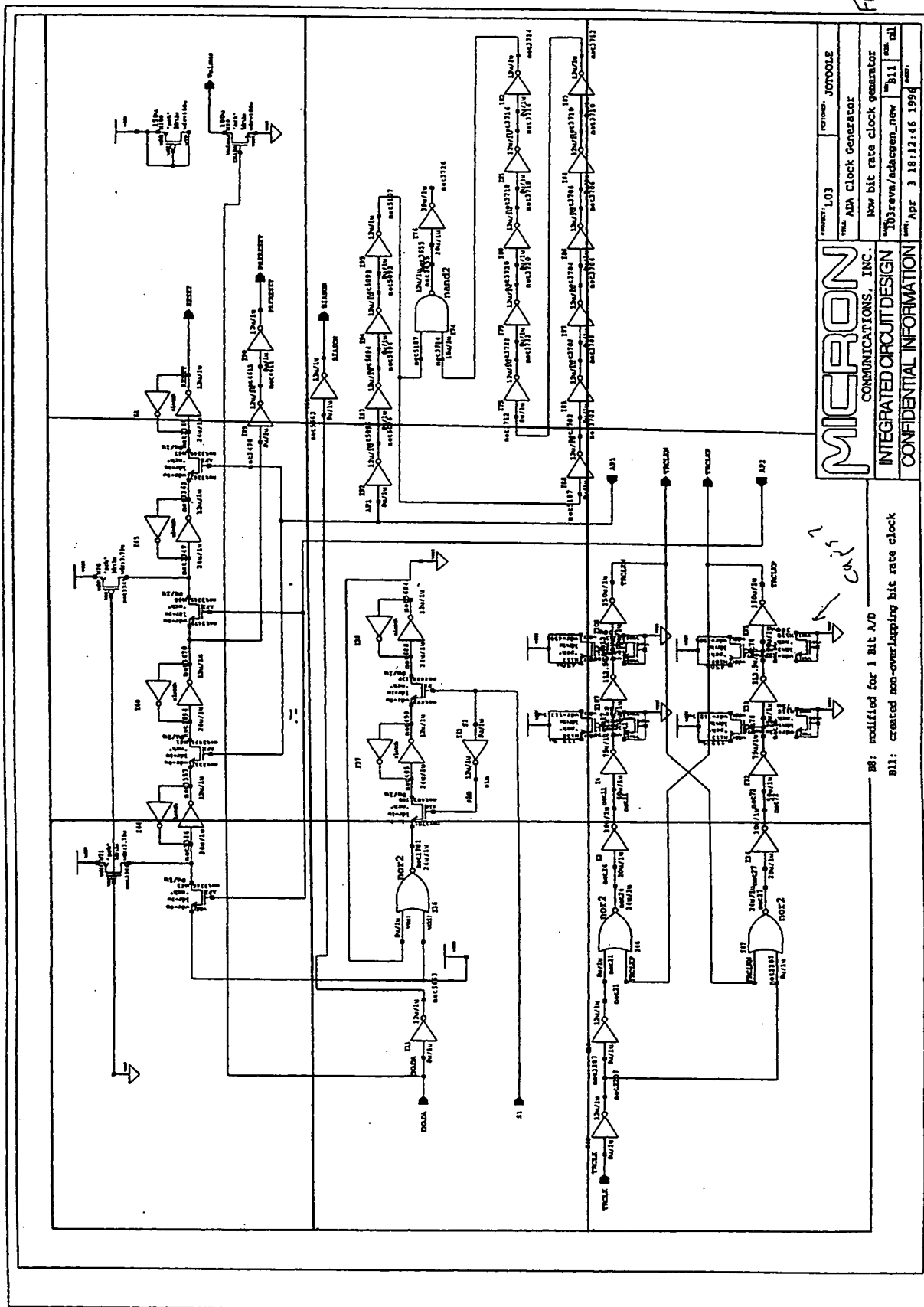
Fig. 9.0103



MICRON  
ELECTRONIC CORPORATION  
10000 N. 10th Ave., Suite 100  
Denver, CO 80231  
Tel: (303) 751-1000  
Fax: (303) 751-1001

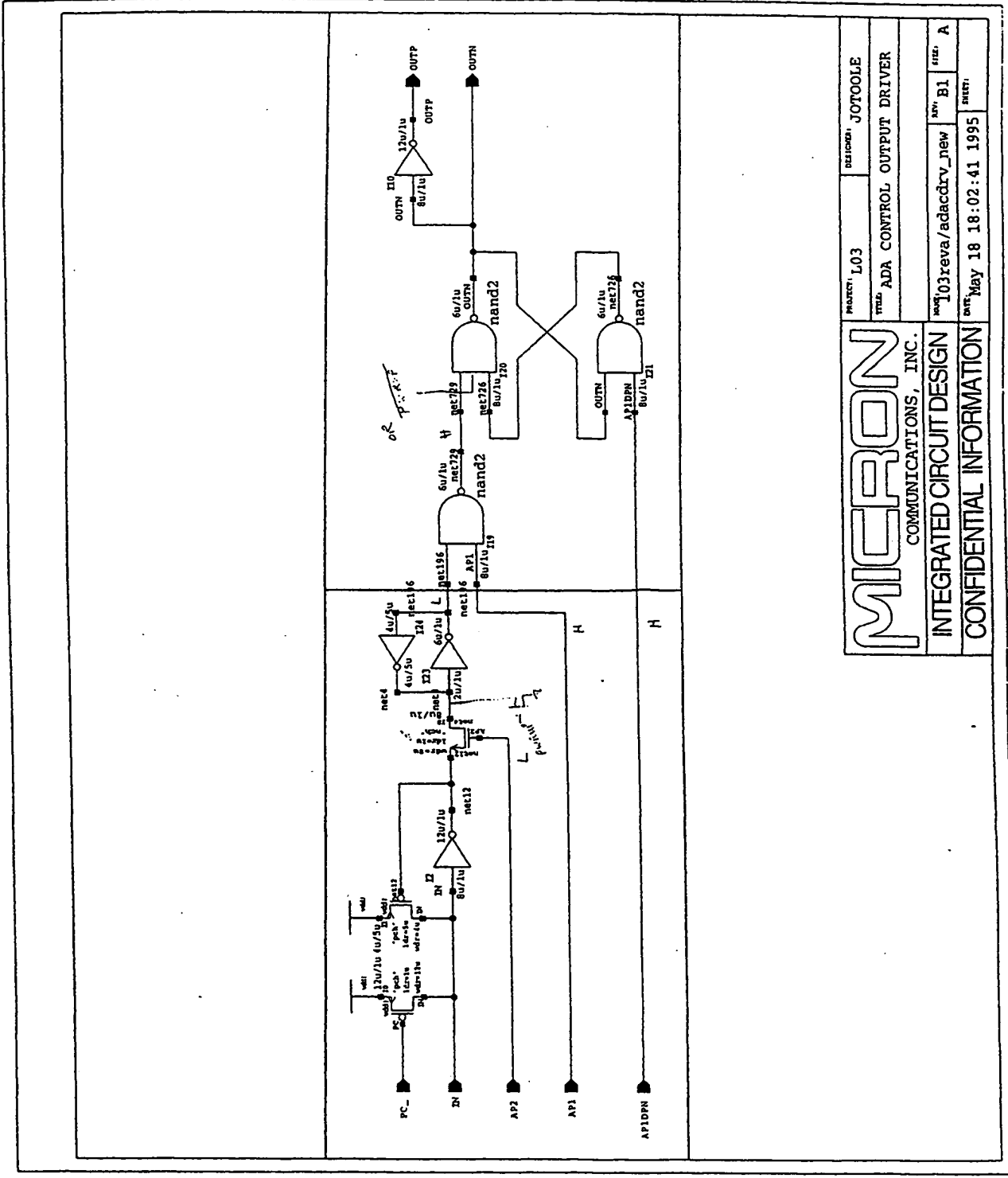
9.010301AA	9.010301AB	9.010301AC
9.010301BA	9.010301BB	9.010301BC
9.010301CA	9.010301CB	9.010301CC

SECRET



9.010302AA	9.010302AB
------------	------------

EX-9010302

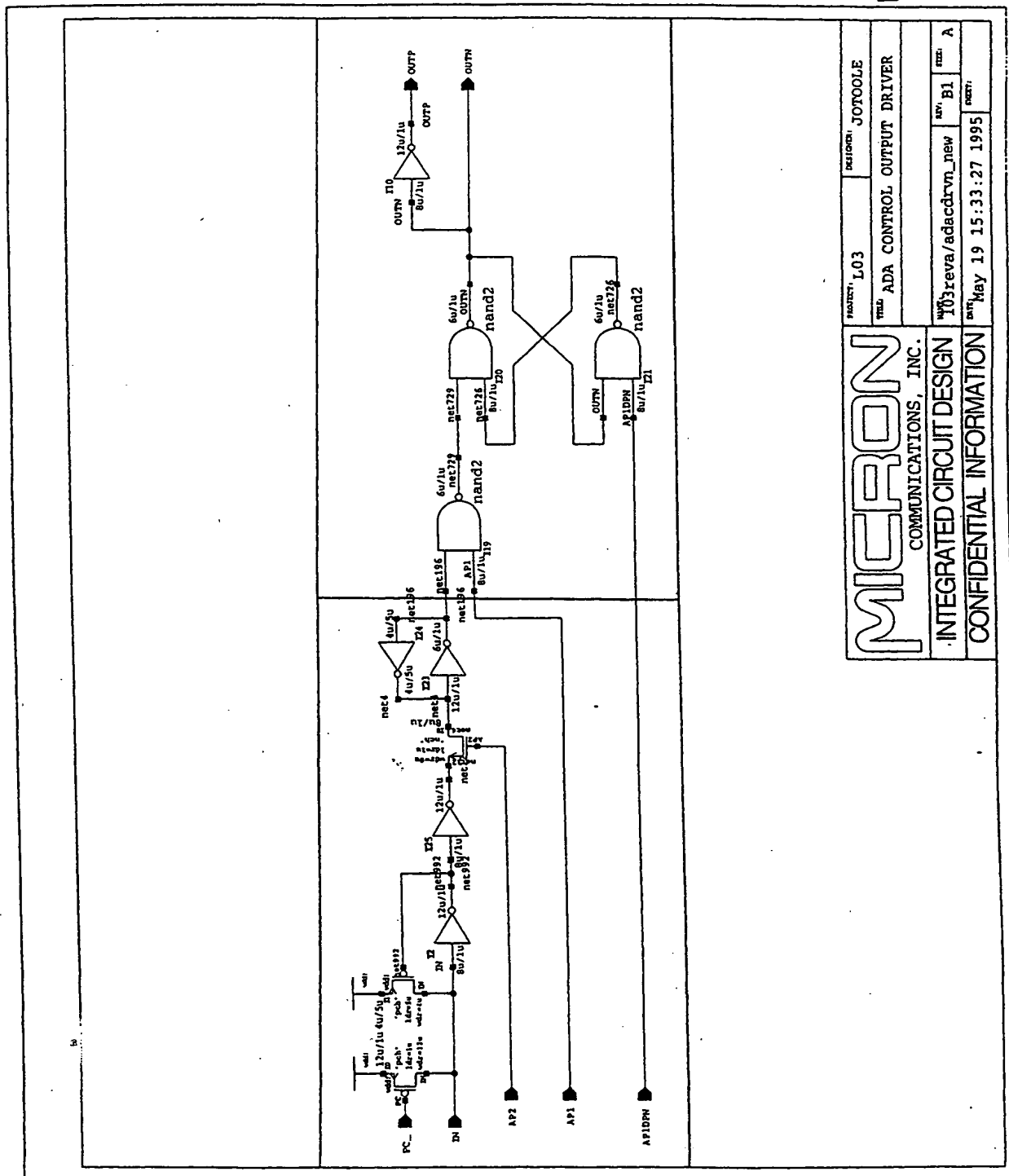


MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: ADA CONTROL OUTPUT DRIVER	
INTEGRATED CIRCUIT DESIGN		DATE: 103reva/adacdrv_new	REV: B1
CONFIDENTIAL INFORMATION		DATE: May 18 18:02:41 1995	REV: A

FIG. 9.010302

9.010303AA	9.010303AB
------------	------------

9.010303

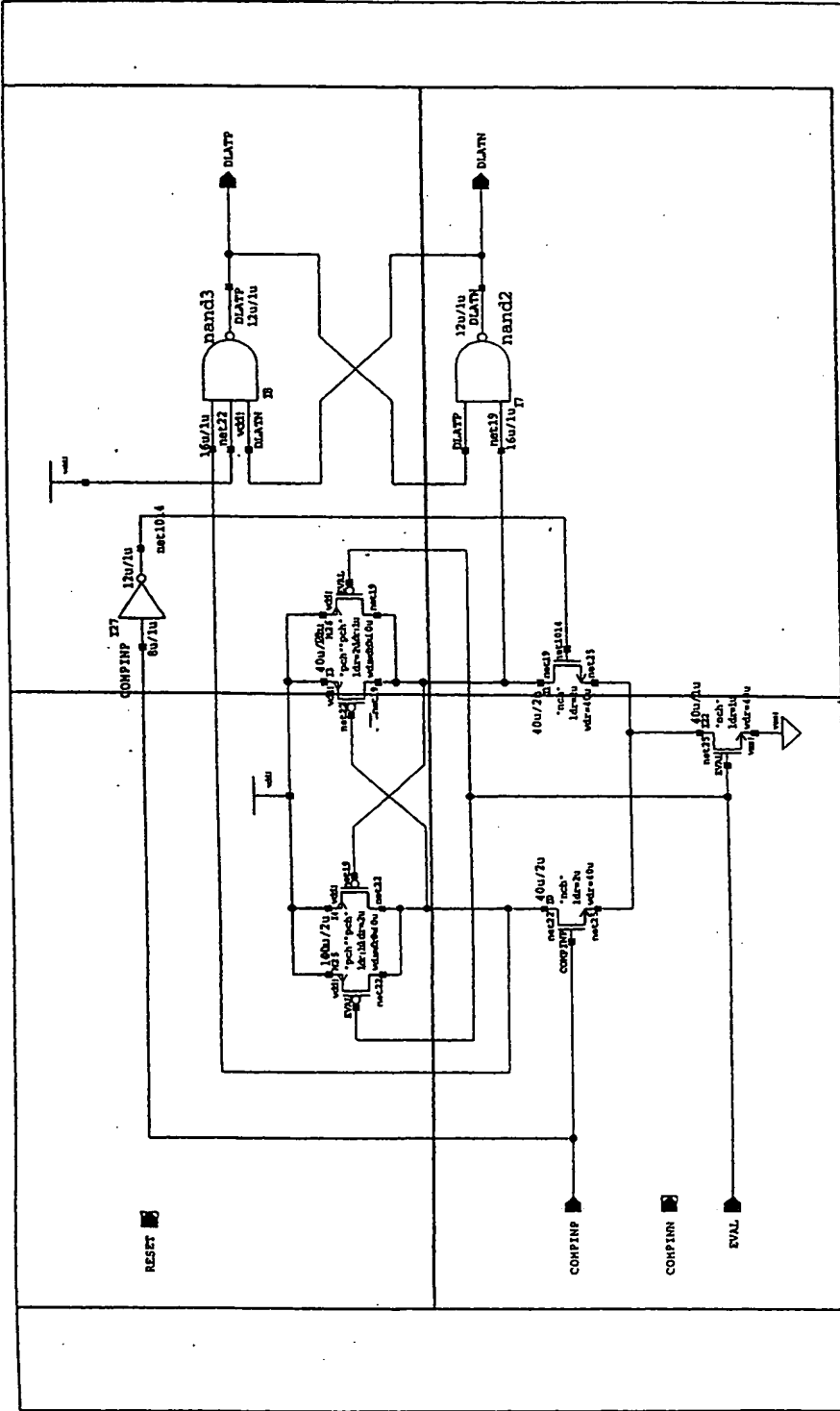




9.010304AB	9.010304BB
9.010304AA	9.010304BA

9.010304

Fig. 9.010304



- B5: disconnect eval input; connect to vss
- B8: reconnect eval and change reset polarity
- B11: modified for use in battery voltage sensor

<b>MICRON</b>		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: ADA Data Latch	
INTEGRATED CIRCUIT DESIGN		REV: B11	DATE: A
CONFIDENTIAL INFORMATION		DATE: Apr 8 10:39:12 1996	DESIGNER: JOTOOLE

9.0104AA	9.0104AB	9.0104AC	9.0104AD	9.0104AE
9.0104BA	9.0104BB	9.0104BC	9.0104BD	9.0104BE
9.0104CA	9.0104CB	9.0104CC	9.0104CD	
9.0104DA	9.0104DB	9.0104DC	9.0104DD	

EX-901104



9.02AA	9.02AB	9.02AC	9.02AD	9.02AE	9.02AF	9.02AG	9.02AH	9.02AI	9.02AJ	9.02AK
9.02BA	9.02BB	9.02BC	9.02BD	9.02BE	9.02BF	9.02BG	9.02BH	9.02BI	9.02BJ	9.02BK
9.02CA		9.02CC	9.02CD	9.02CE	9.02CF	9.02CG	9.02CH	9.02CI	9.02CJ	9.02CK
9.02DA	9.02DB	9.02DC	9.02DD		9.02DF	9.02DG	9.02DH	9.02DI	9.02DJ	9.02DK

11.11.11 09.11.11

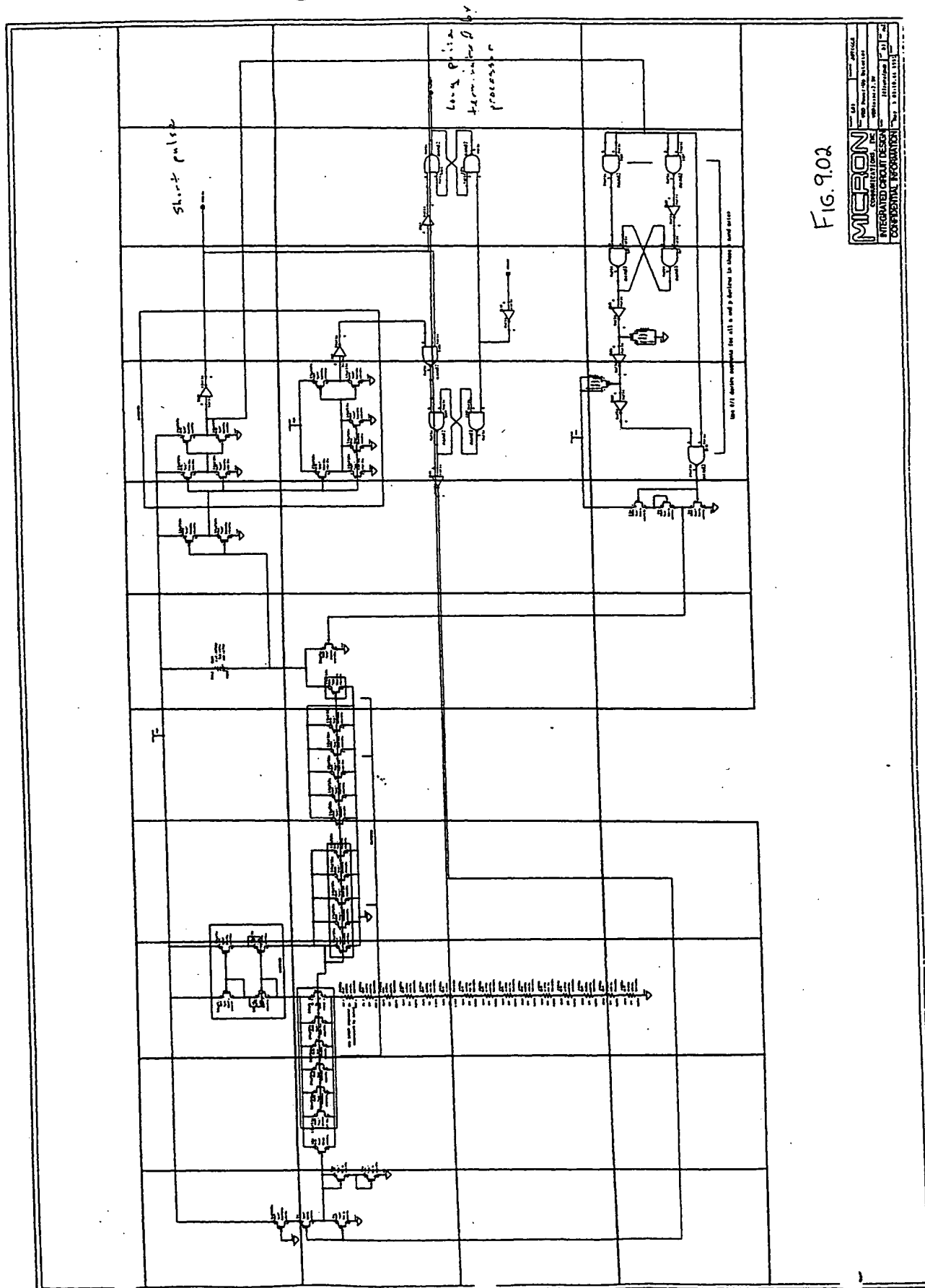
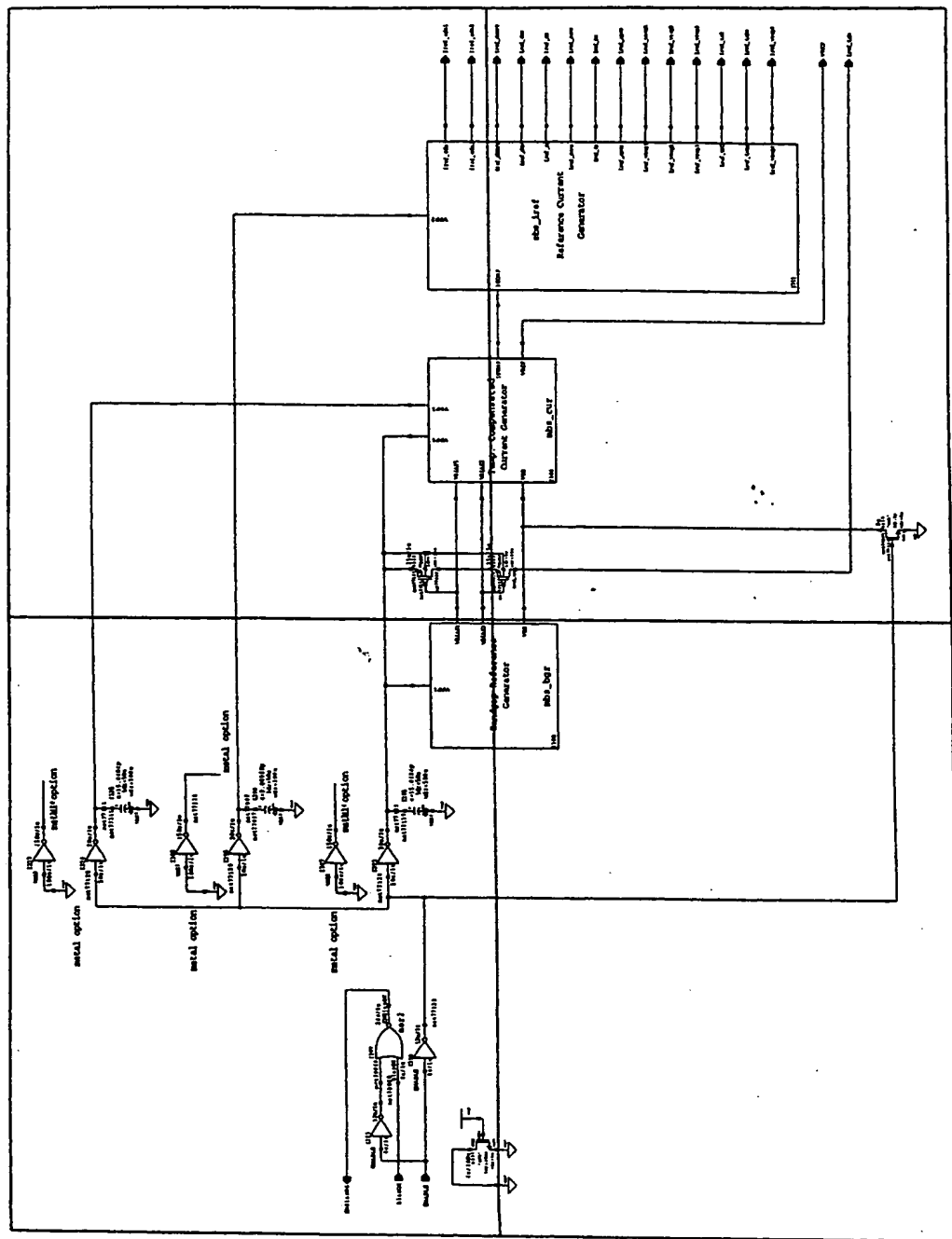


FIG. 9.02

9.03AA	9.03AB
9.03BA	9.03BB

9.03

FIG. 9.03



02: deleted TESTING function  
added DBMSOK logic  
created buffered VDI

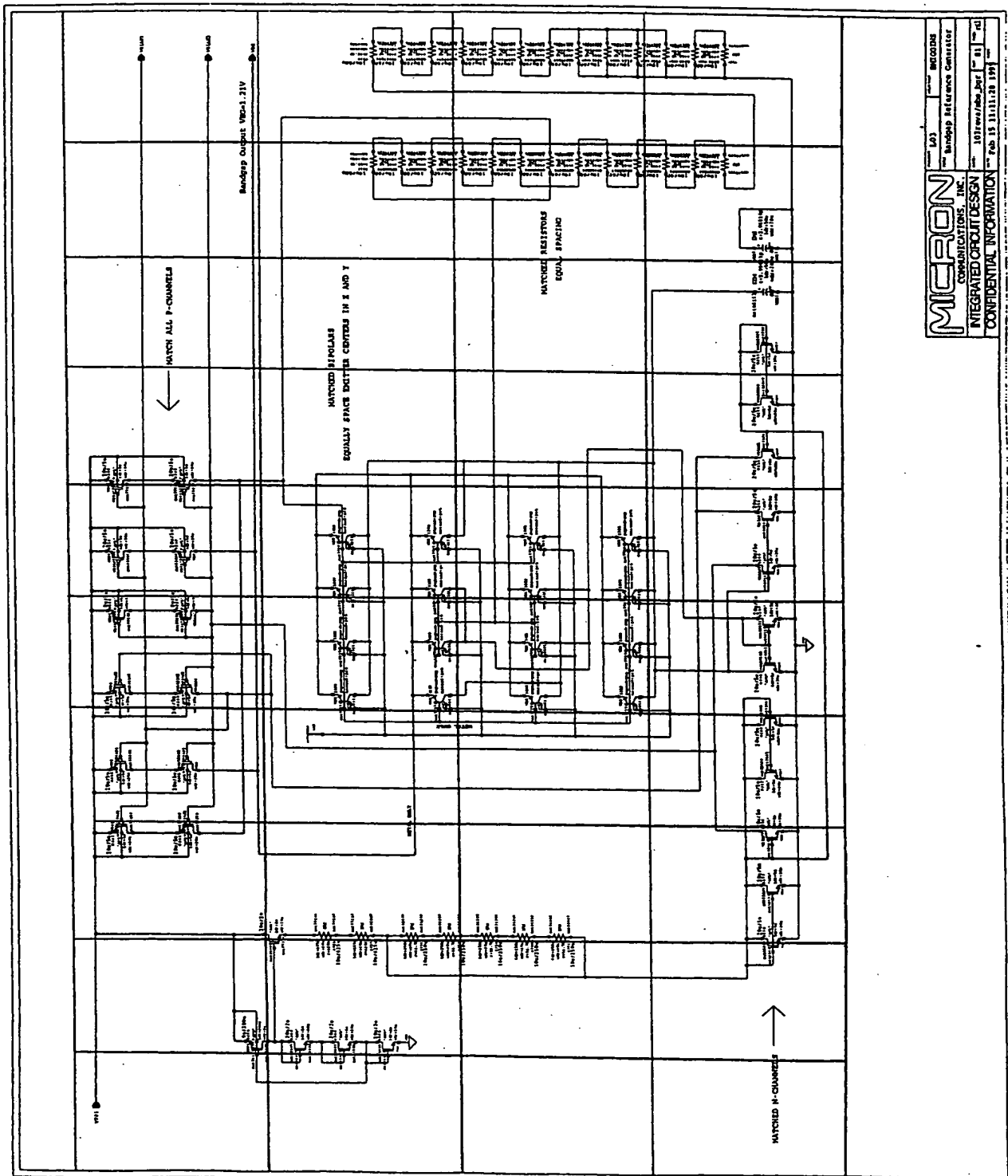
MICRON		L03		MICROFILMS	
COMMUNICATIONS, INC.		Hester Blue Source			
INTEGRATED CIRCUIT DESIGN					
CONFIDENTIAL INFORMATION		1032raw/mbe		32 - all	
		JUL 28 11:00:13 1995			



9.0301AA	9.0301AB	9.0301AC	9.0301AD	9.0301AE	9.0301AF	9.0301AG	9.0301AH	9.0301AI	9.0301AJ
9.0301BA	9.0301BB	9.0301BC	9.0301BD	9.0301BE	9.0301BF	9.0301BG	9.0301BH	9.0301BI	9.0301BJ
	9.0301CB	9.0301CC	9.0301CD	9.0301CE	9.0301CF	9.0301CG	9.0301CH	9.0301CI	9.0301CJ
	9.0301DB	9.0301DC	9.0301DD	9.0301DE	9.0301DF	9.0301DG	9.0301DH	9.0301DI	9.0301DJ

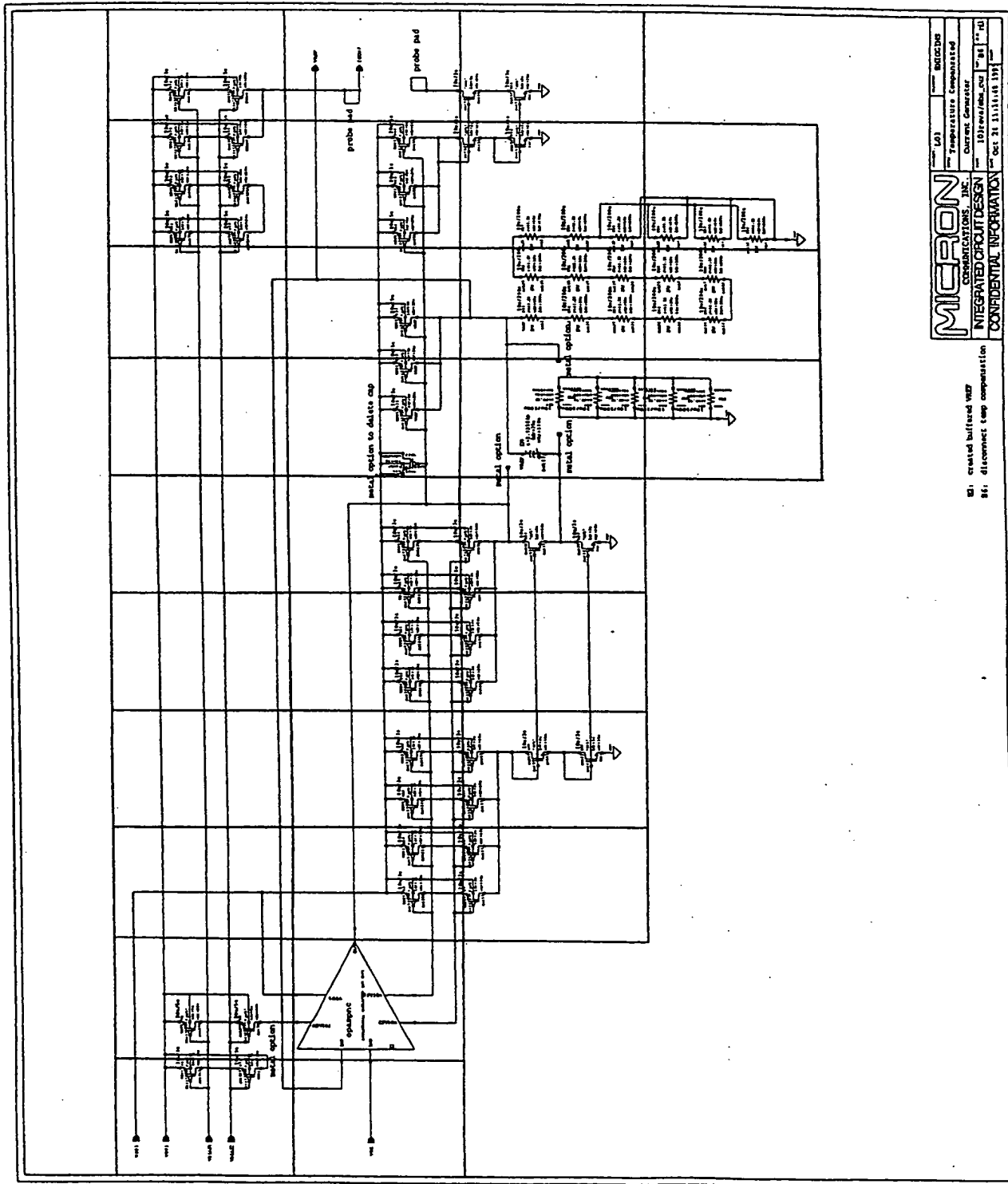



FIG. 9.0301



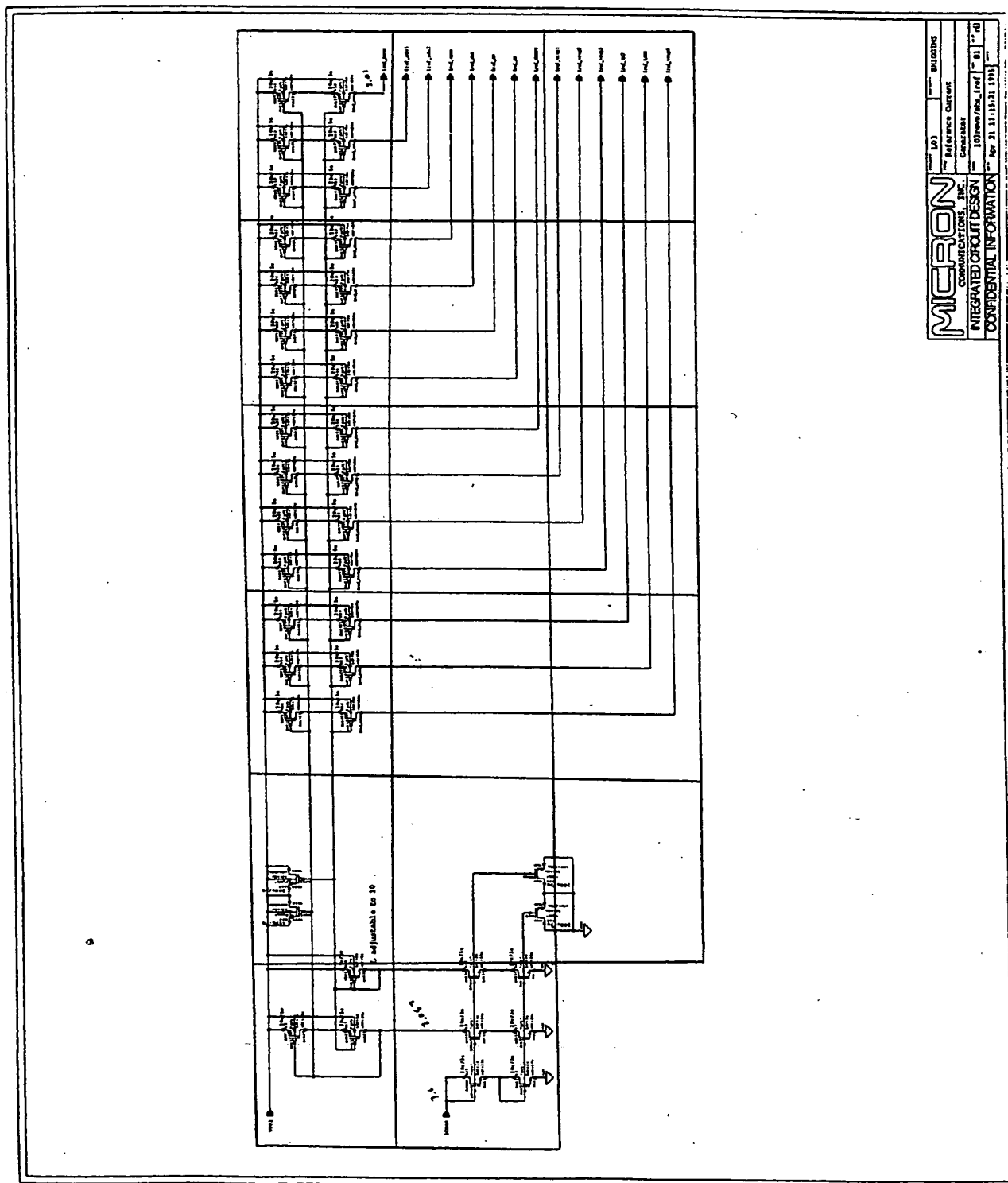
9.0302AA	9.0302AB	9.0302AC	9.0302AD	9.0302AE	9.0302AF	9.0302AG	9.0302AH	9.0302AI	9.0302AJ
9.0302BA	9.0302BB	9.0302BC	9.0302BD	9.0302BE	9.0302BF	9.0302BG	9.0302BH	9.0302BI	9.0302BJ
		9.0302CC	9.0302CD	9.0302CE	9.0302CF	9.0302CG	9.0302CH	9.0302CI	9.0302CJ
								9.0302DI	

EE 9.0302



9.0303AA	9.0303AB	9.0303AC	9.0303AD	9.0303AE	9.0303AF
9.0303BA	9.0303BB	9.0303BC	9.0303BD	9.0303BE	9.0303BF
	9.0303CB	9.0303CC	9.0303CD	9.0303CE	9.0303CF

FEENE'S



9.04AA	9.04AB	9.04AC	9.04AD	9.04AE
9.04BA	9.04BB	9.04BC	9.04BD	9.04BE
9.04CA	9.04CB	9.04CC	9.04CD	9.04CE

EX 9.04

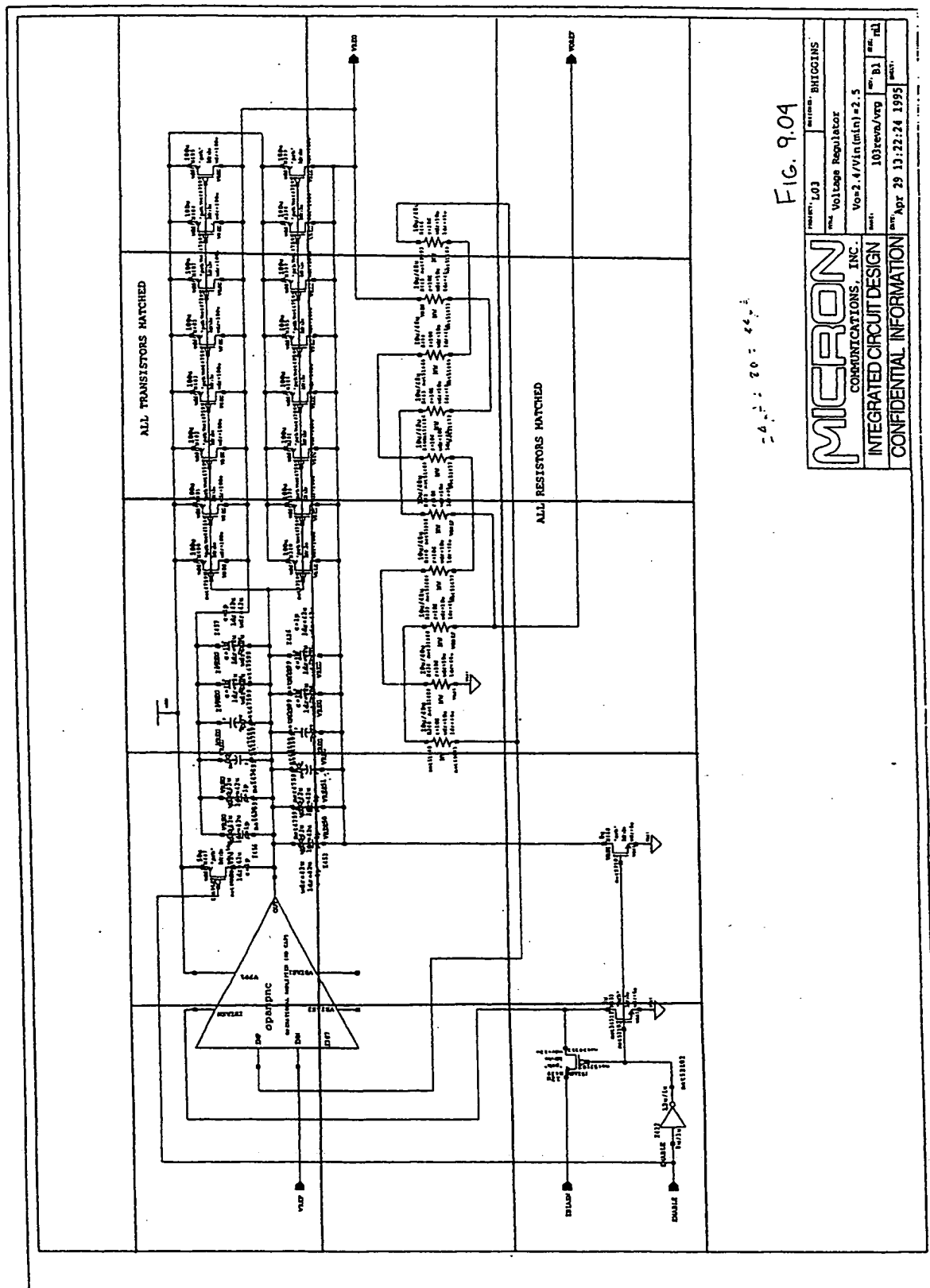


FIG. 9.04

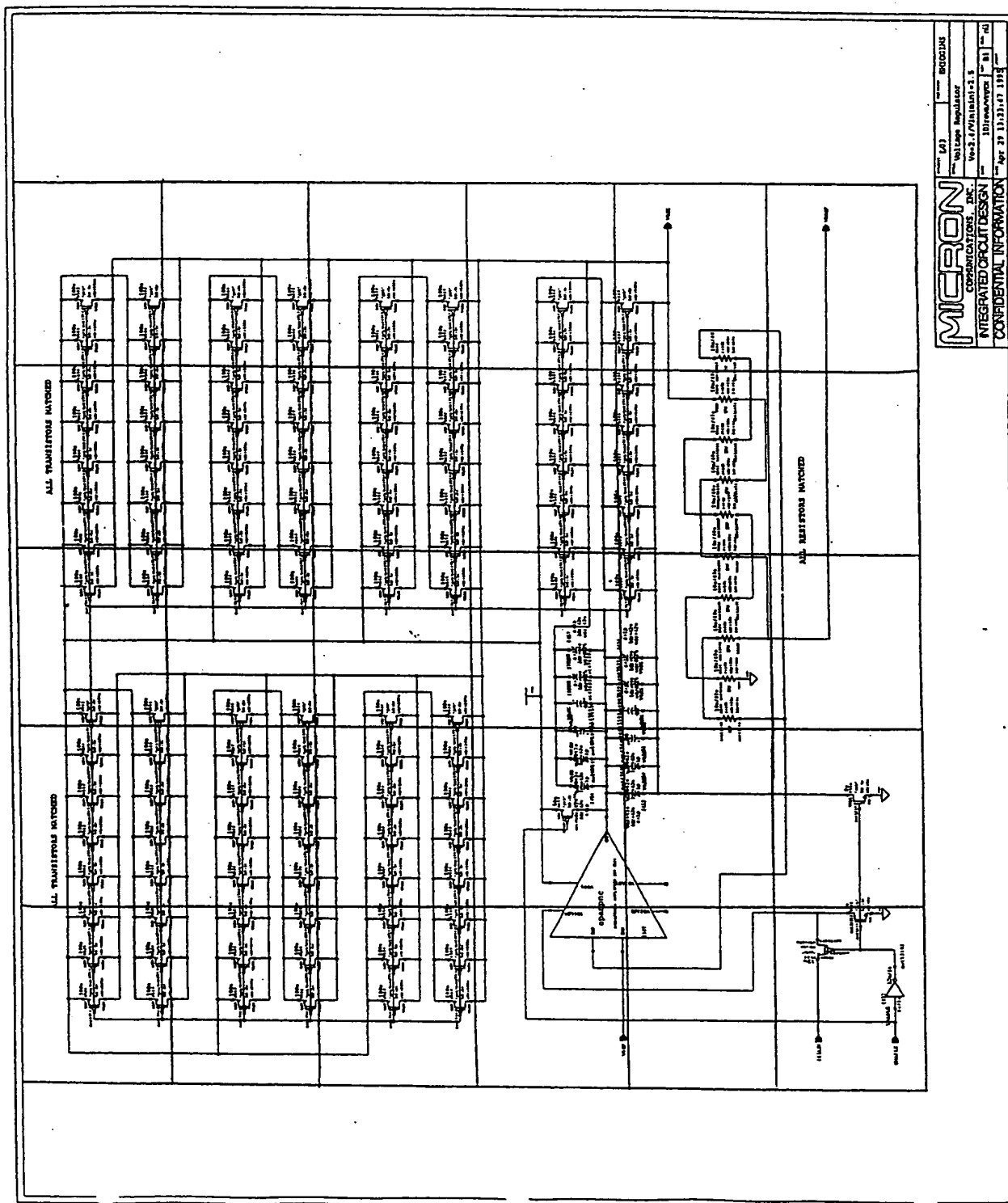
MICRON		PROJECT: L03	DESIGNER: BHTIGGINS
COMMUNICATIONS, INC.		Title: Voltage Regulator	
INTEGRATED CIRCUIT DESIGN		V <sub>0</sub> =2.4V/in (min)=2.5	
CONFIDENTIAL INFORMATION		103revs/vrp	
		DATE: Apr 29 13:22:24 1995	



9.05AA	9.05AB	9.05AC	9.05AD	9.05AE
9.05BA	9.05BB	9.05BC	9.05BD	9.05BE
9.05CA	9.05CB	9.05CC	9.05CD	9.05CE
9.05DA	9.05DB	9.05DC	9.05DD	9.05DE
9.05EA	9.05EB	9.05EC	9.05ED	9.05EE
9.05FA	9.05FB	9.05FC	9.05FD	9.05FE

II II 99.005

Fig. 9.05



9.0501AA	9.0501AB	9.0501AC	9.0501AD
9.0501BA	9.0501BB	9.0501BC	9.0501BD
9.0501CA	9.0501CB	9.0501CC	9.0501CD

IL 9.0501

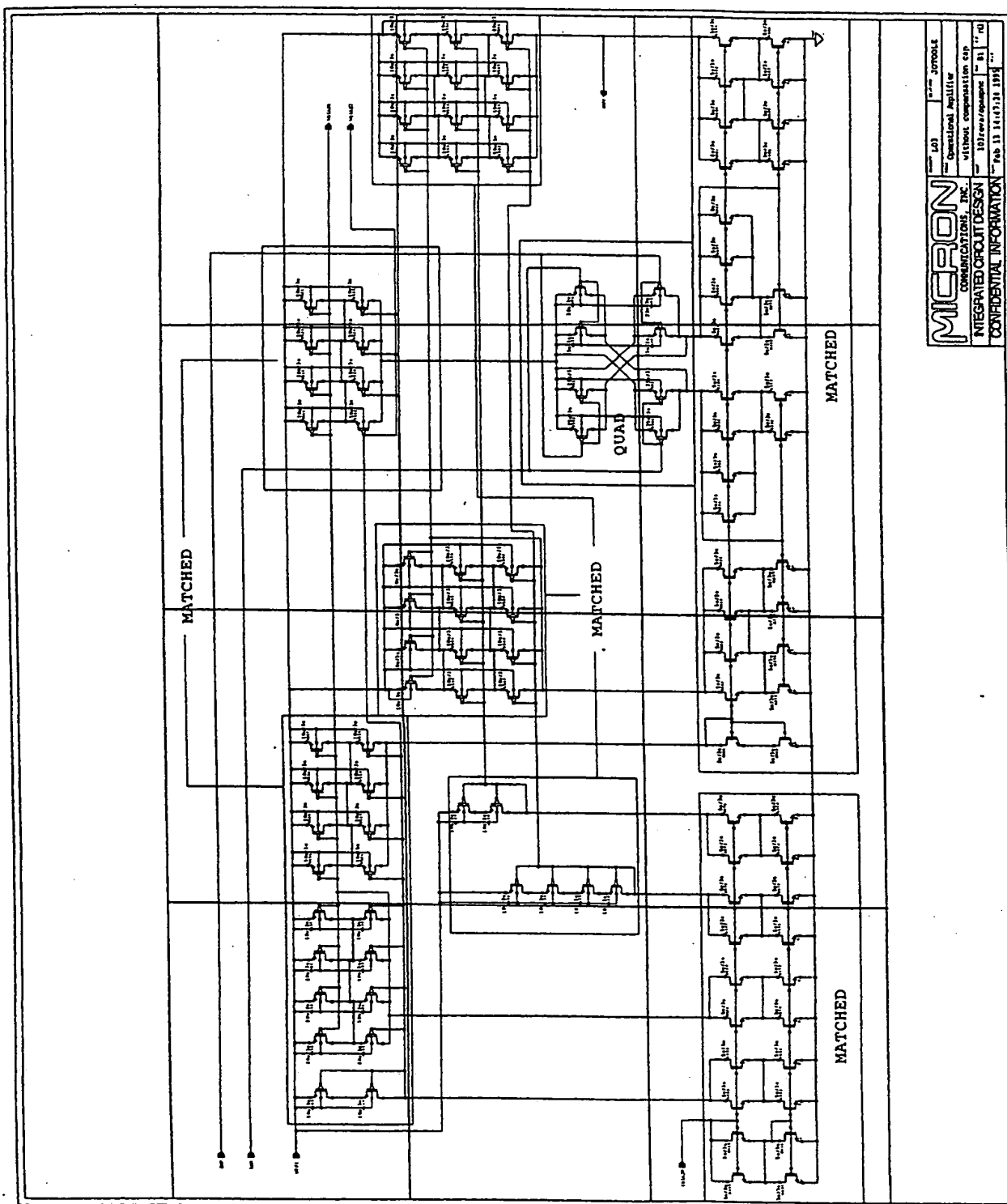
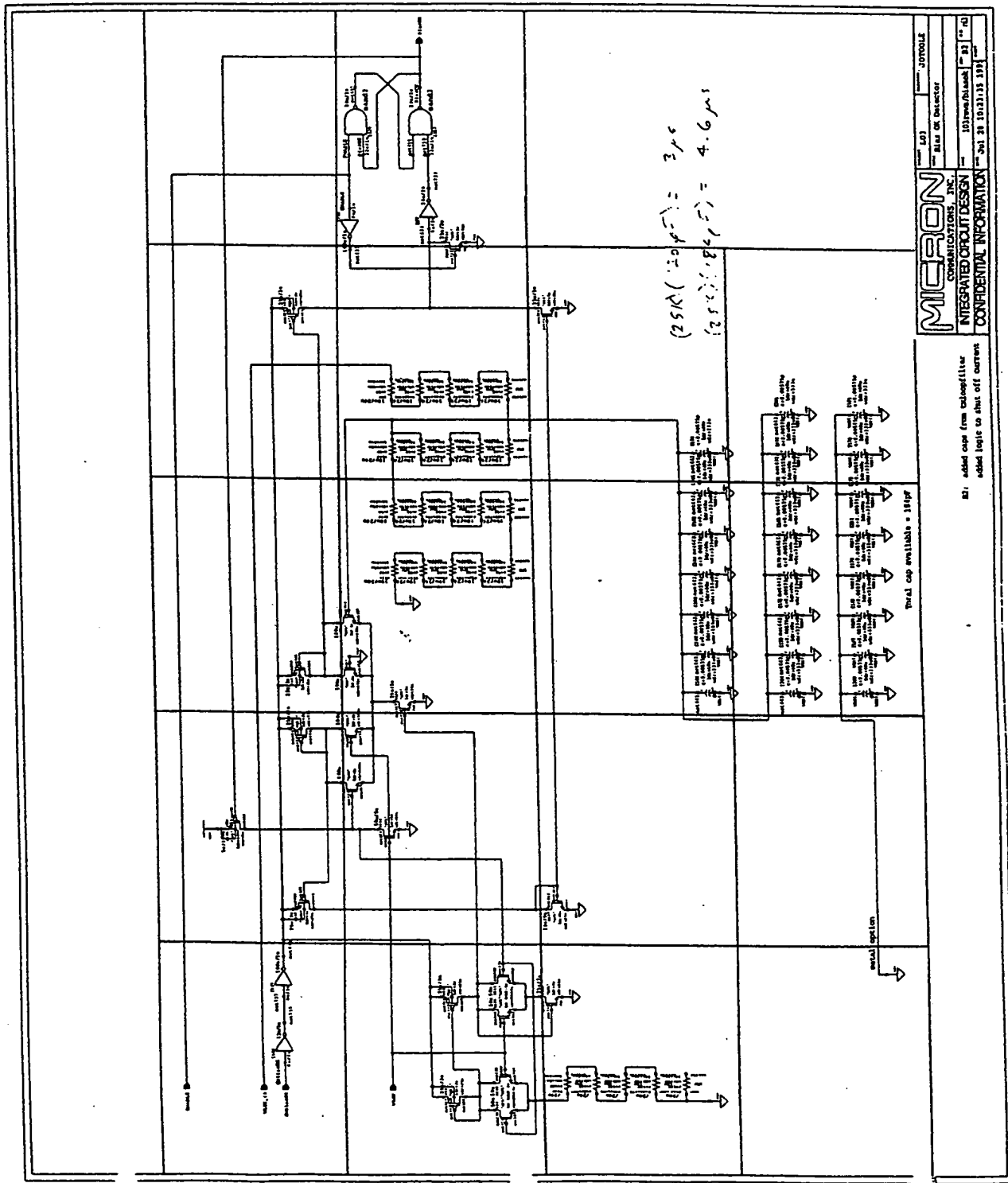


Fig. 9.0501

9.06AA	9.06AB	9.06AC	9.06AD	9.06AE
9.06BA	9.06BB	9.06BC	9.06BD	9.06BE
9.06CA	9.06CB	9.06CC	9.06CD	
9.06DA	9.06DB	9.06DC	9.06DD	

SECRET

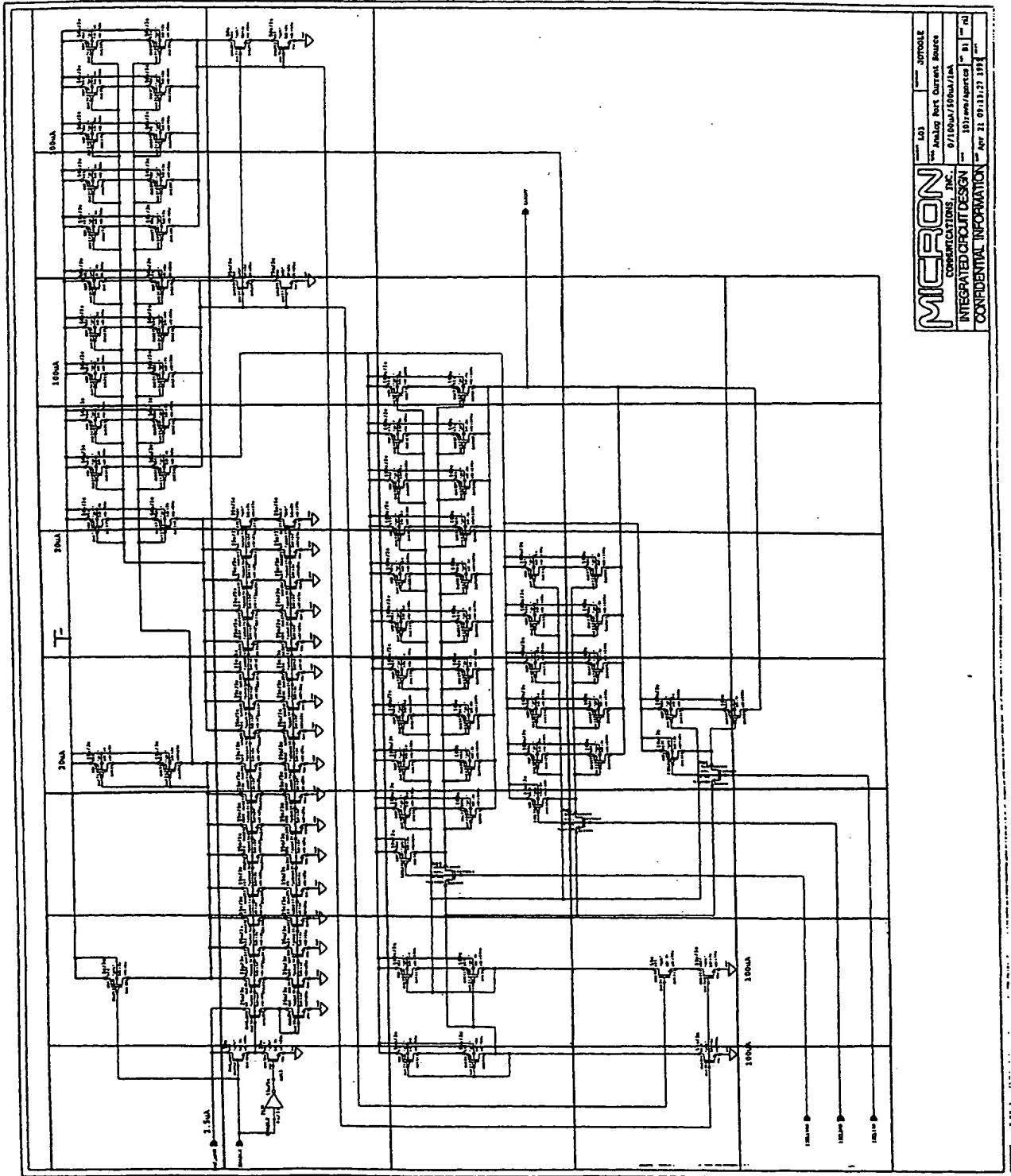
Fig. 9.06



9.07AA	9.07AB	9.07AC	9.07AD	9.07AE	9.07AF	9.07AG	9.07AH	9.07AI
9.07BA	9.07BB	9.07BC	9.07BD	9.07BE	9.07BF	9.07BG	9.07BH	9.07BI
9.07CA	9.07CB	9.07CC	9.07CD	9.07CE	9.07CF	9.07CG	9.07CH	
9.07DA	9.07DB	9.07DC	9.07DD	9.07DE	9.07DF	9.07DG		
9.07EA	9.07EB	9.07EC	9.07ED	9.07EE	9.07EF	9.07EG		

SECRET

FIG. 9.07



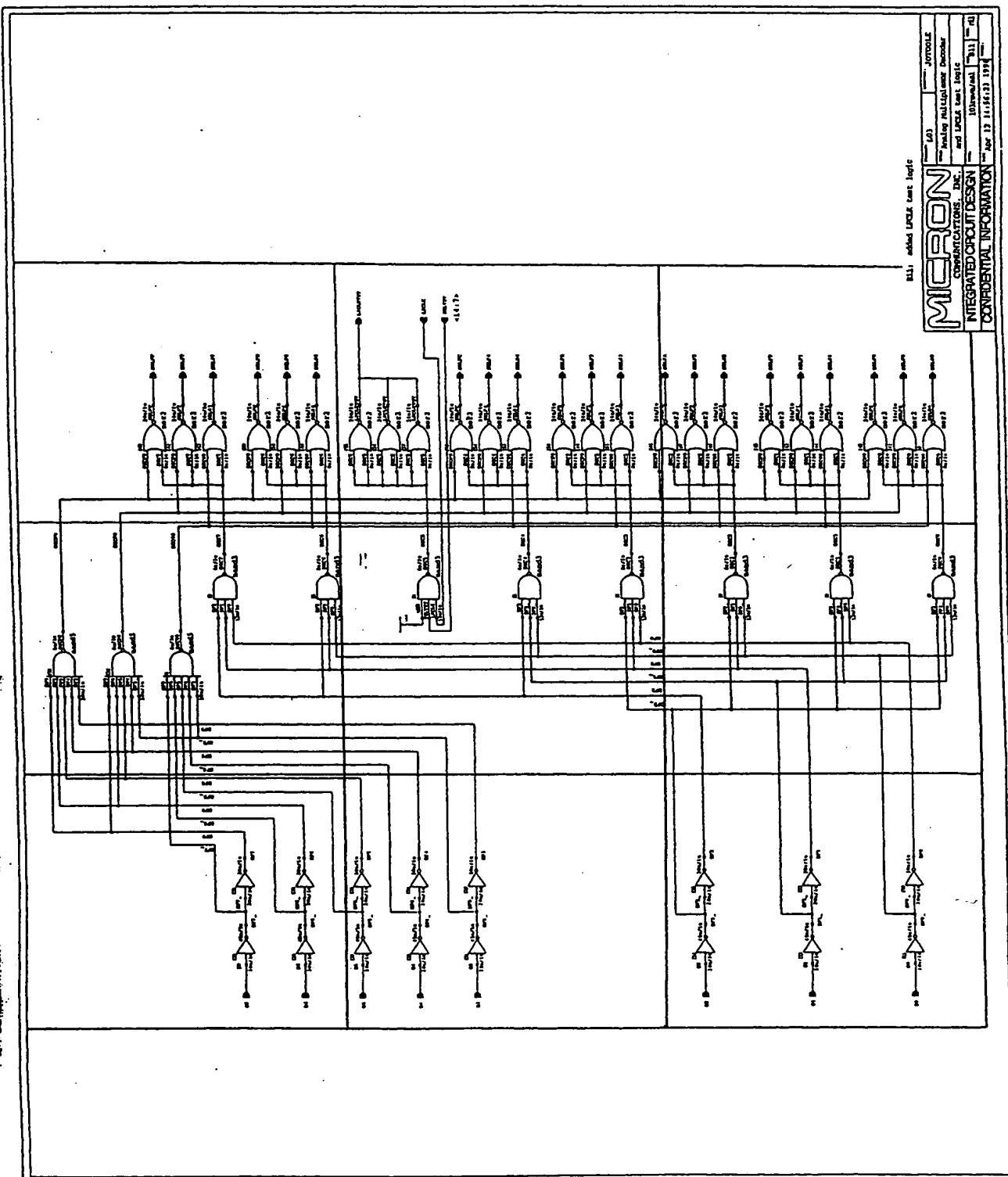
<b>MICRON</b>		DESIGN	DATE
INTEGRATED CIRCUIT DESIGN		01/10/83	01/10/83
CONFIDENTIAL INFORMATION		01/10/83	01/10/83
CONFIDENTIAL INFORMATION		01/10/83	01/10/83



9.08AA	9.08AB	9.08AC
9.08BA	9.08BB	9.08BC
9.08CA	9.08CB	9.08CC

II II 9.08B

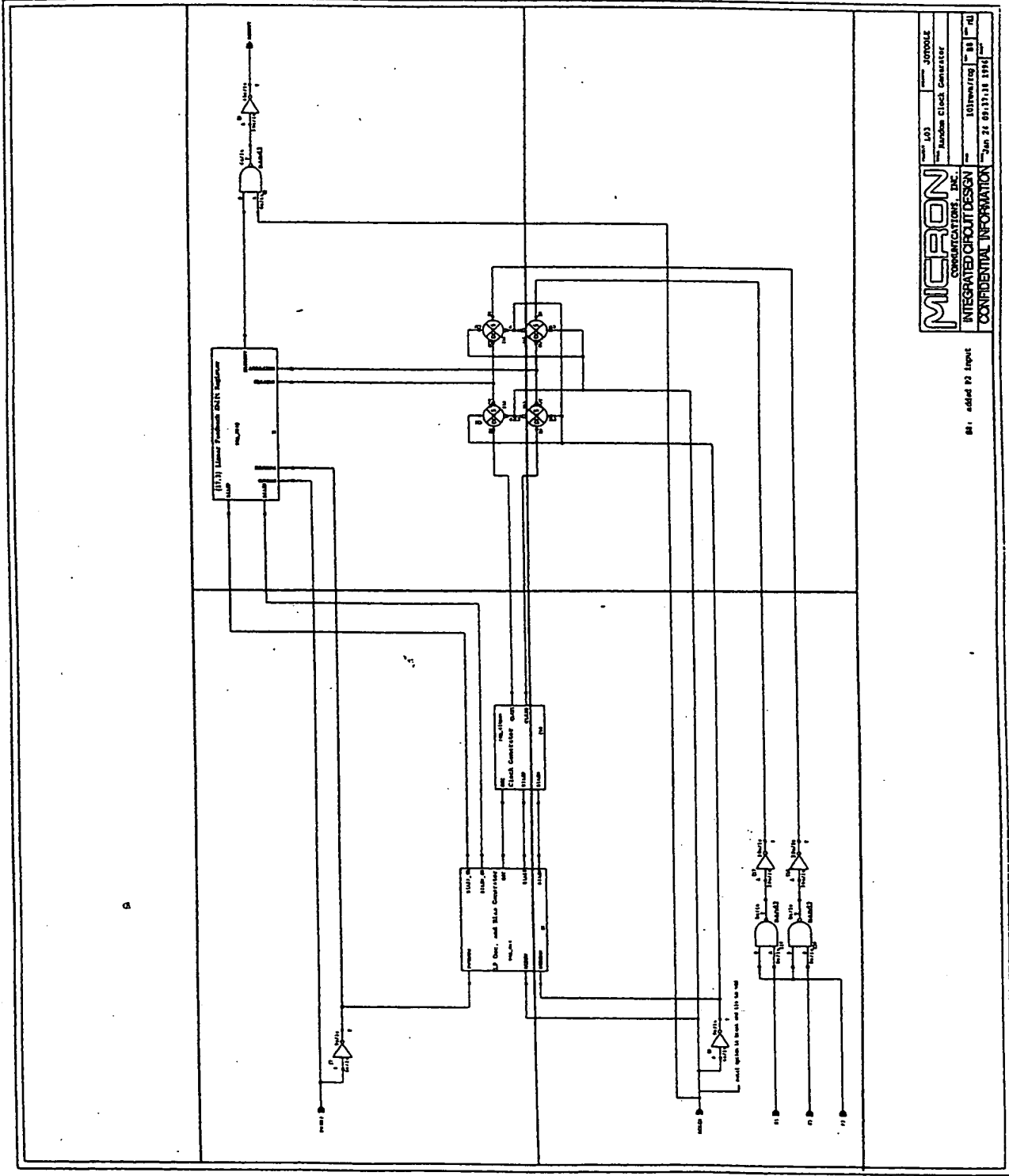
<b>MICRON</b>		COMMUNICATIONS, INC.	
INTEGRATED CIRCUIT DESIGN			
CONFIDENTIAL INFORMATION			
LAD		JORDALE	
Issuing Multiple-use Decoder		10/28/88	
and LAPCA Test Logic		Page 12 of 16, 23, 1988	



9.09AA	9.09AB
9.09BA	9.09BB

EX-9.09

Fig. 9.09



<b>MICRON</b>		MODEL 103	NAME J070014
CONFIDENTIAL		Random Clock Controller	
INTEGRATED CIRCUIT DESIGN		101revs/07	81
CONFIDENTIAL INFORMATION		Jan 22 09:17:18 1982	70

81: added 32 Input

9.0901AA	9.0901AB	9.0901AC	9.0901AD	9.0901AE	9.0901AF	9.0901AG	9.0901AH
9.0901BA	9.0901BB	9.0901BC	9.0901BD	9.0901BE	9.0901BF	9.0901BG	9.0901BH
9.0901CA	9.0901CB	9.0901CC	9.0901CD	9.0901CE	9.0901CF	9.0901CG	9.0901CH

EX 9.0901

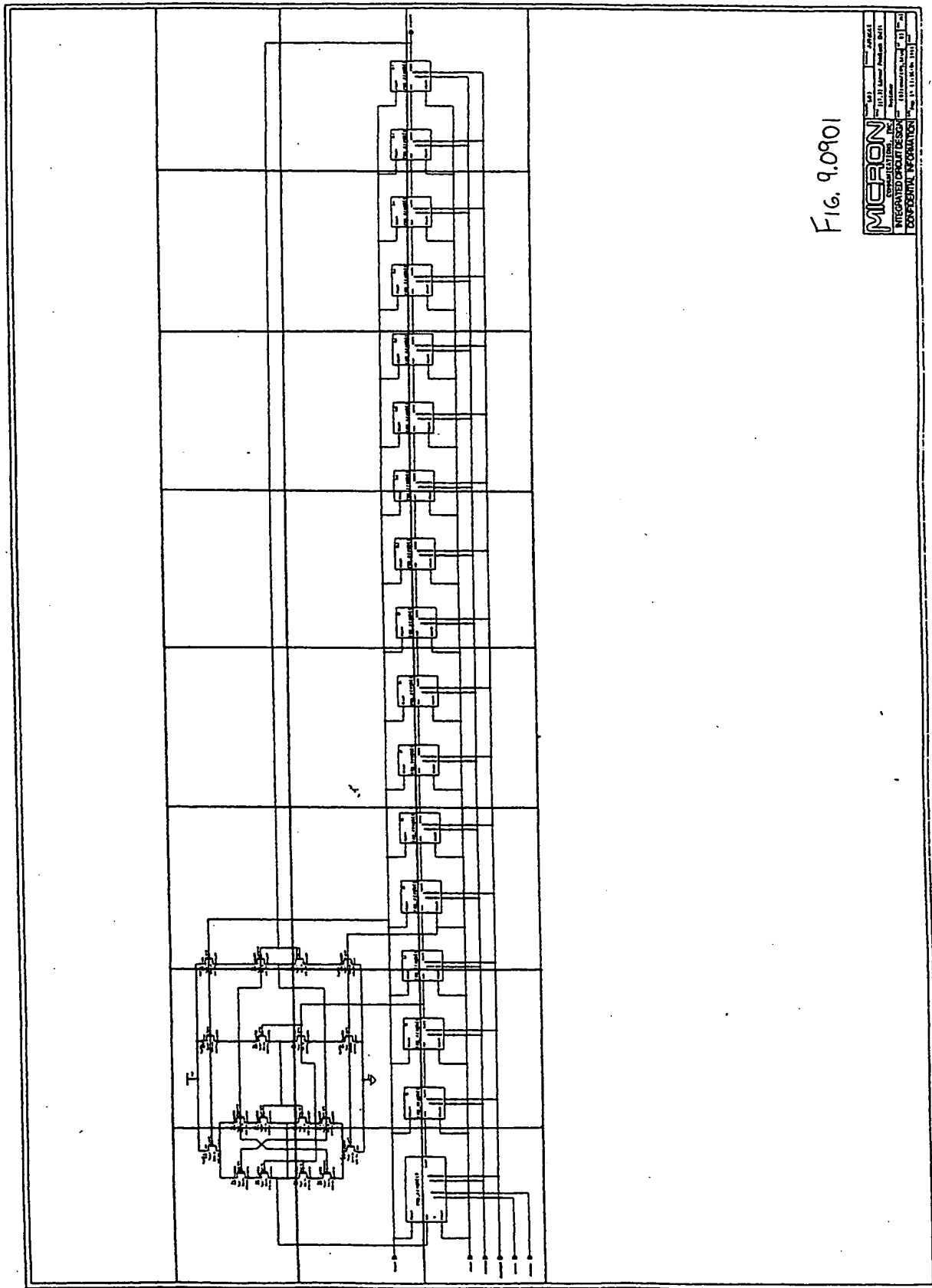


Fig. 9.0901

9.090101AA	9.090101AB	9.090101AC
9.090101BA	9.090101BB	9.090101BC
9.090101CA	9.090101CB	9.090101CC

II II II II II II II II

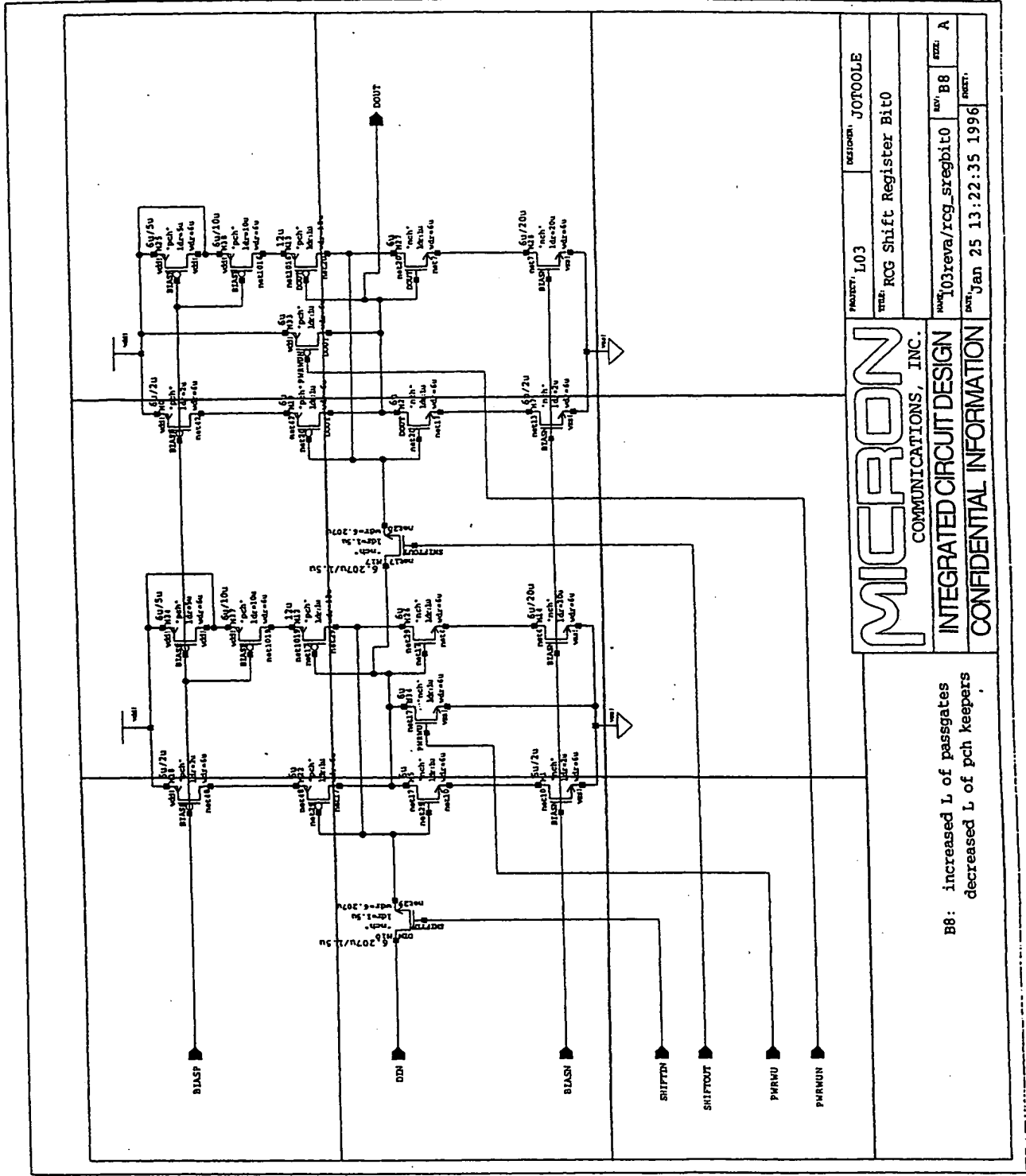


FIG. 9.090101

MICRON		PROJECT: L03	DESIGNER: JOT00LE
COMMUNICATIONS, INC.		TITLE: RCG Shift Register Bit0	
INTEGRATED CIRCUIT DESIGN		NAME: j03:eva/rcg_sregbit0	REV: B8
CONFIDENTIAL INFORMATION		DATE: Jan 25 13:22:35 1996	SIZE: A

B8: increased L of passgates  
decreased L of pch keepers



9.090102AA	9.090102AB
9.090102BA	9.090102BB

EX 9.090102

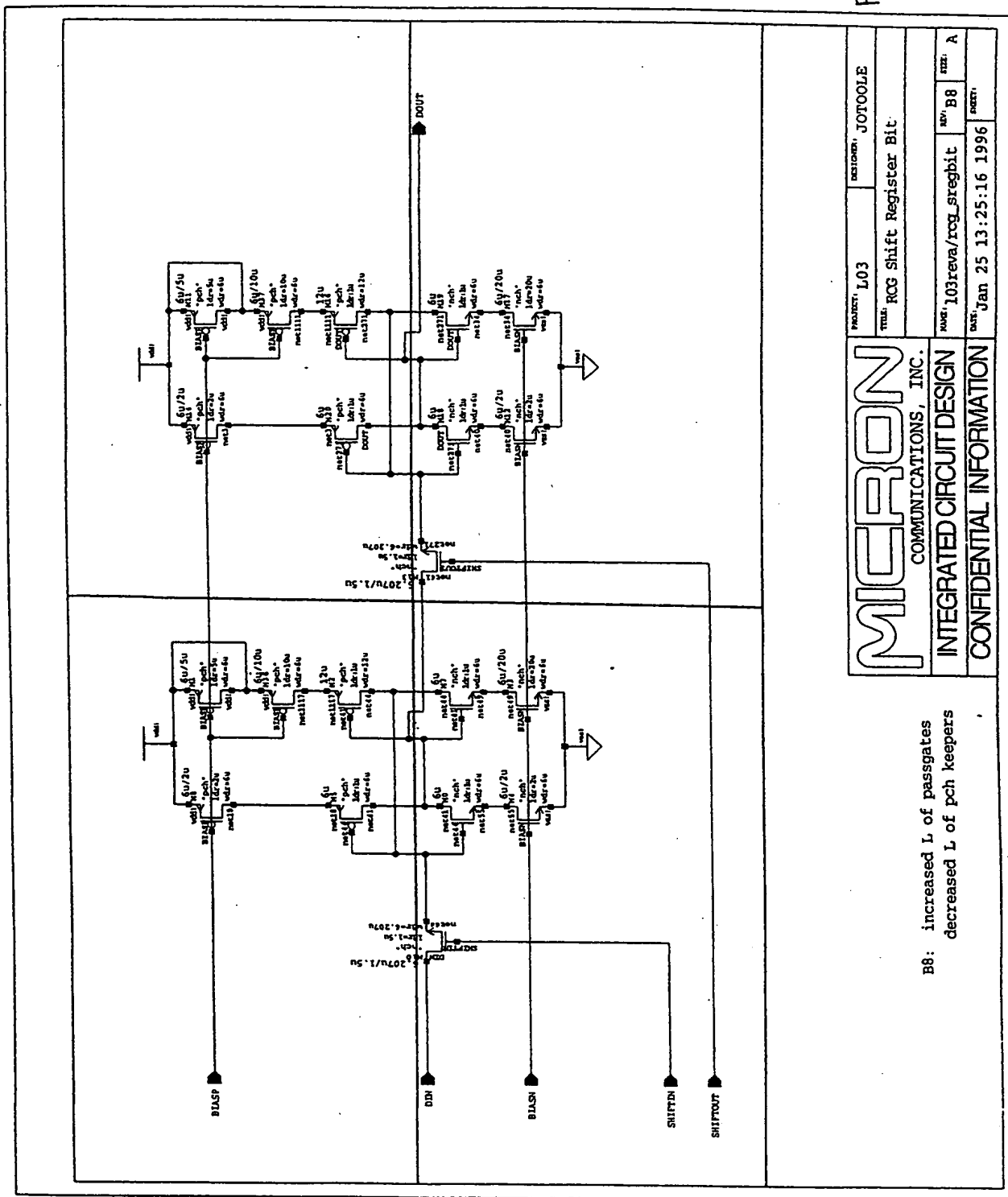
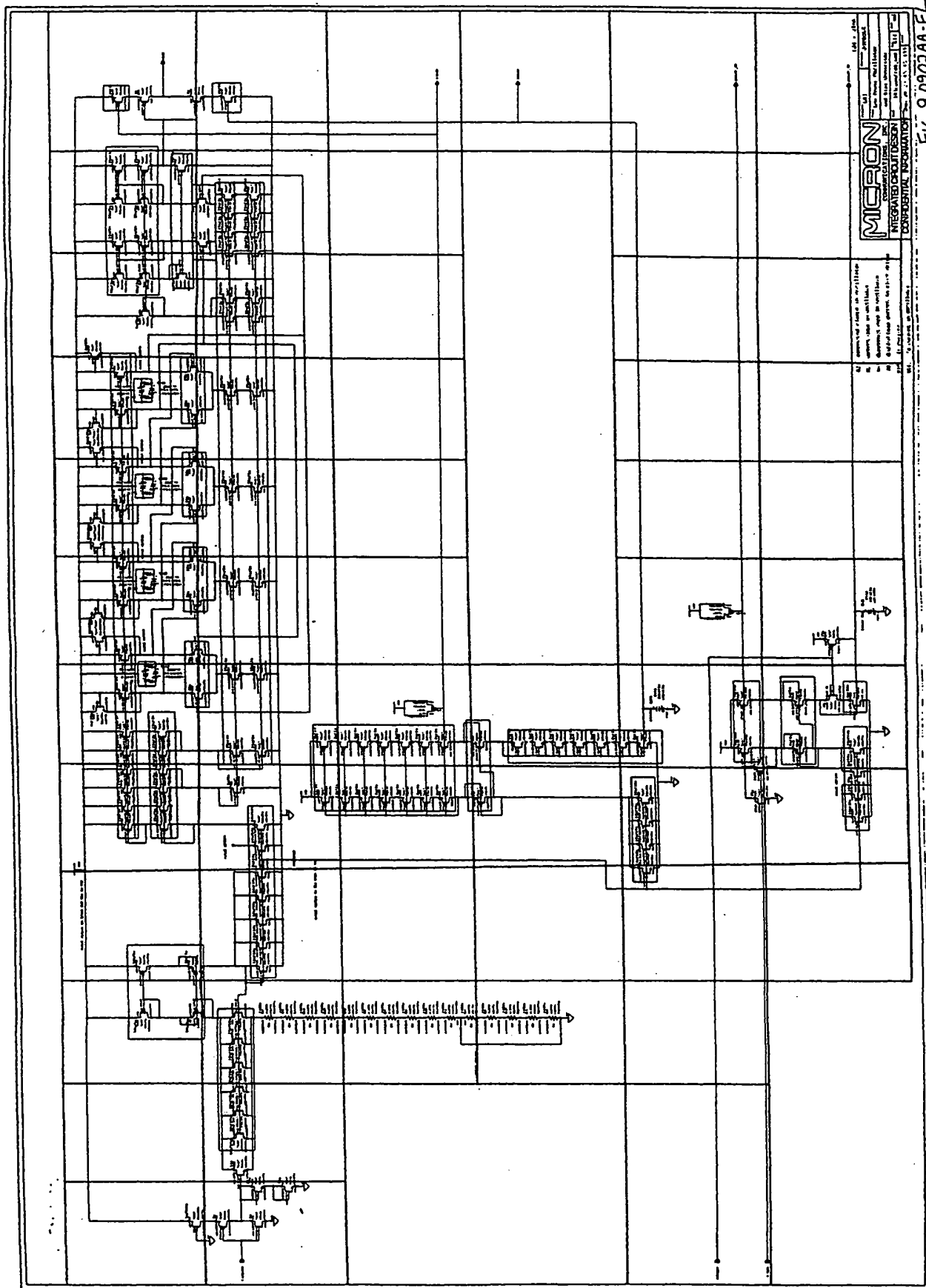


Fig. 9.090102

9.0902AA	9.0902AB	9.0902AC	9.0902AD	9.0902AE	9.0902F	9.0902AG	9.0902AH	9.0902AI	9.0902AJ	9.0902AK	9.0902AL
9.0902BA	9.0902BB	9.0902BC	9.0902BD	9.0902BE	9.0902F	9.0902BG	9.0902BH	9.0902BI	9.0902BJ	9.0902BK	9.0902BL
		9.0902CC	9.0902CD	9.0902CE	9.0902F	9.0902CG	9.0902CH	9.0902CI	9.0902CJ	9.0902CK	9.0902CL
		9.0902DC	9.0902DD	9.0902DE	9.0902F						9.0902DL
9.0902EA	9.0902EB	9.0902EC	9.0902ED	9.0902EE	9.0902F	9.0902EG	9.0902EH	9.0902EI	9.0902EJ	9.0902EK	9.0902EL
			9.0902FD	9.0902FE	9.0902F	9.0902FG	9.0902FH	9.0902FI	9.0902FJ	9.0902FK	9.0902FL

II II 9.0902



**MICRON**  
 CORPORATION  
 8000 NE 28TH AVE.  
 BOCA RATON, FL 33433  
 (305) 395-1000

FIG. 9.0903AA-F

9.0903AA	9.0903AB	9.0903AC
9.0903BA	9.0903BB	9.0903BC
9.0903CA	9.0903CB	9.0903CC

ILX 9.0903

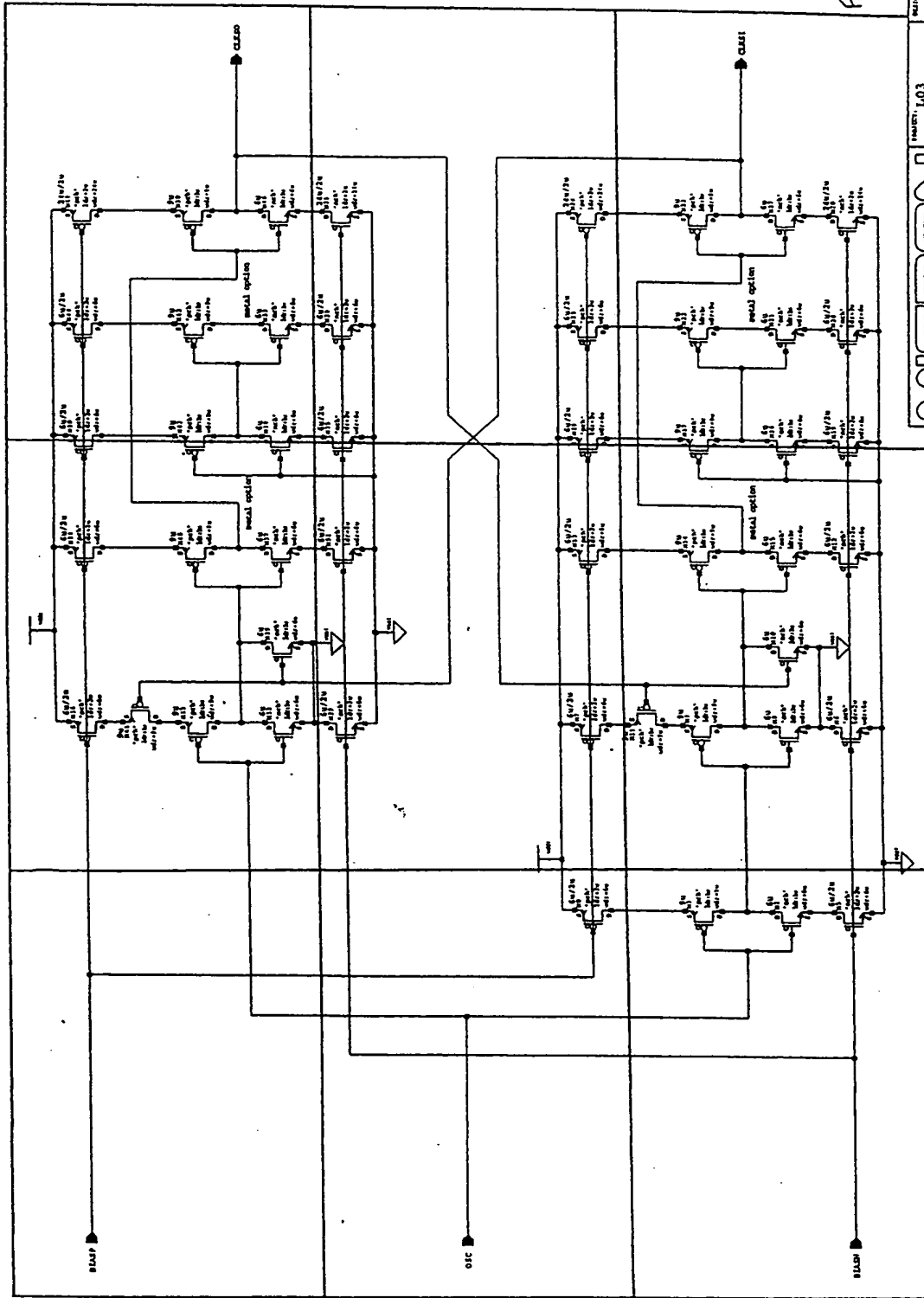


Fig. 9.0903

**MICRON**  
COMMUNICATIONS, INC.

INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

REVISION: L03  
NAME: Clock Generator  
J07000LE

88: wired cross-couples to ground

DATE: 103rev0a/rcq.clkgen  
REV: 88  
JAN 24 09:56:43 1996

10AA	10AB	10AC	10AD
10BA	10BB	10BC	10BD
10CA	10CB	10CC	10CD
10DA	10DB	10DC	10DD

11.11.11





10.01AA	10.01AB	10.01AC	10.01AD	10.01AE	10.01AF	10.01AG			
10.01BA	10.01BB	10.01BC	10.01BD	10.01BE	10.01BF	10.01BG	10.01BH	10.01BI	10.01BJ
10.01CA	10.01CB	10.01CC	10.01CD	10.01CE	10.01CF	10.01CG	10.01CH	10.01CI	10.01CJ
	10.01DB	10.01DC	10.01DD	10.01DE	10.01DF	10.01DG	10.01DH	10.01DI	10.01DJ

II II II II II II

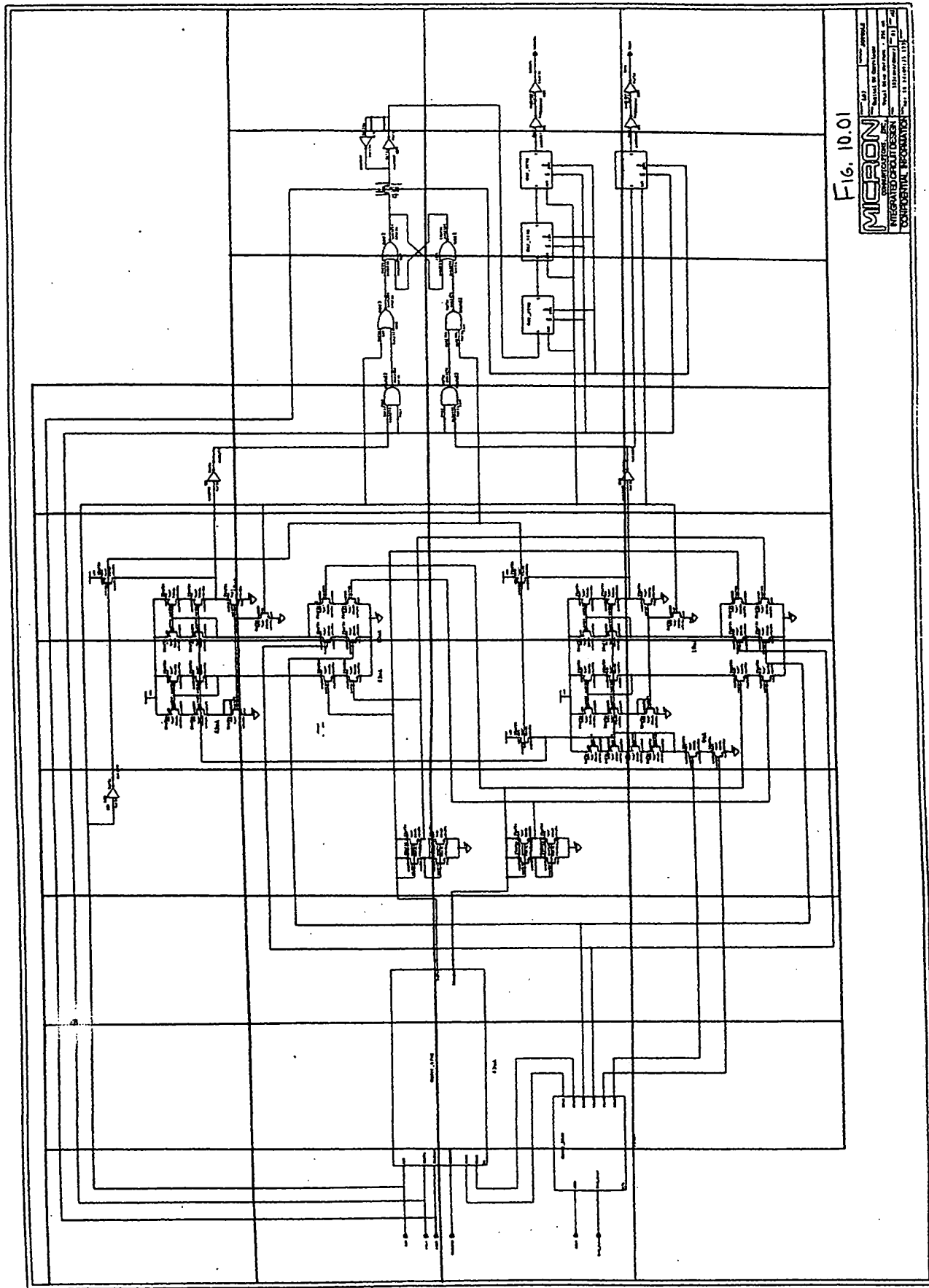


Fig. 10.01

10.0101AA	10.0101AB	10.0101AC	10.0101AD	10.0101AE	10.0101AF	10.0101AG
10.0101BA	10.0101BB	10.0101BC	10.0101BD	10.0101BE	10.0101BF	10.0101BG

10.0101

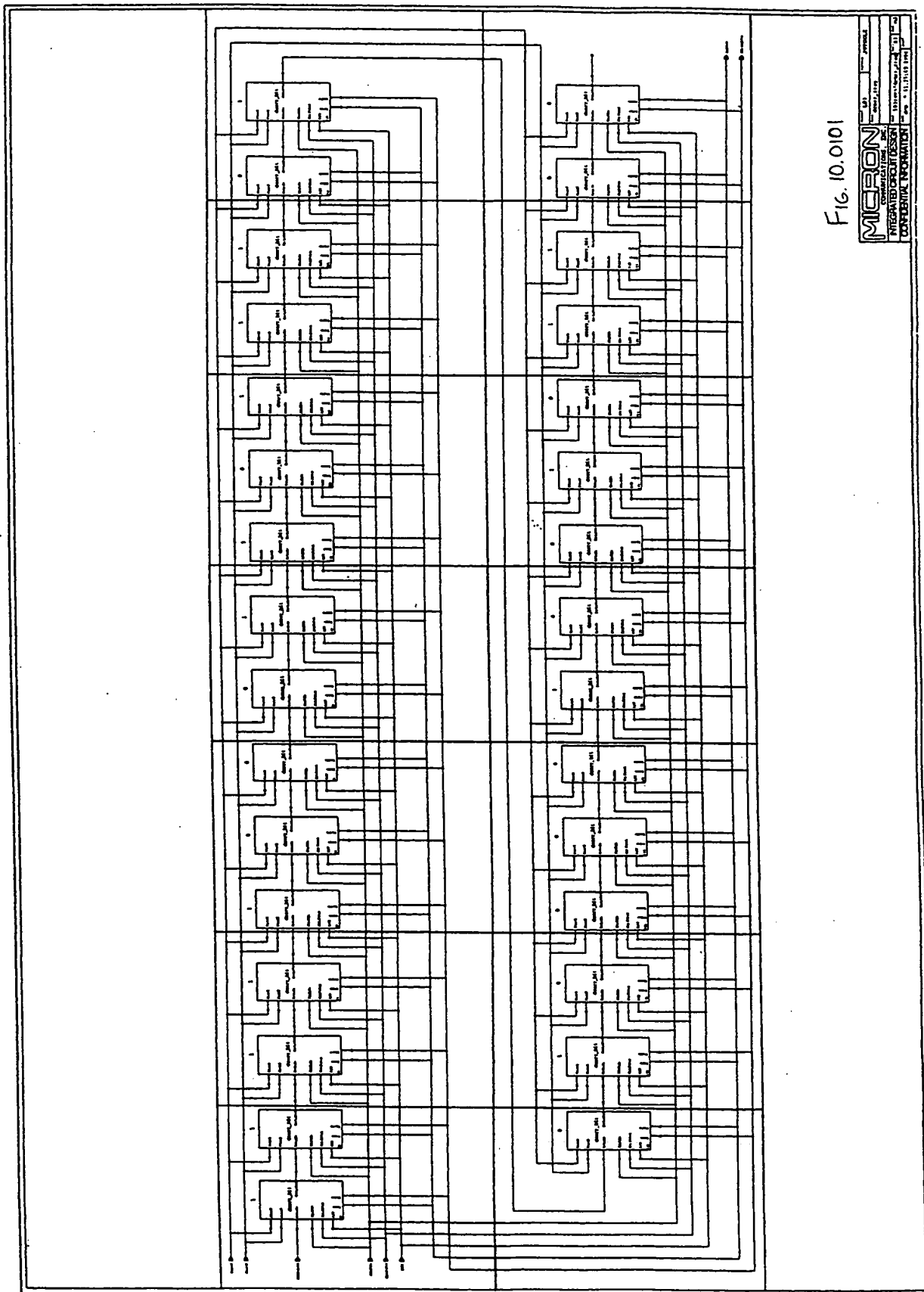


Fig. 10.0101

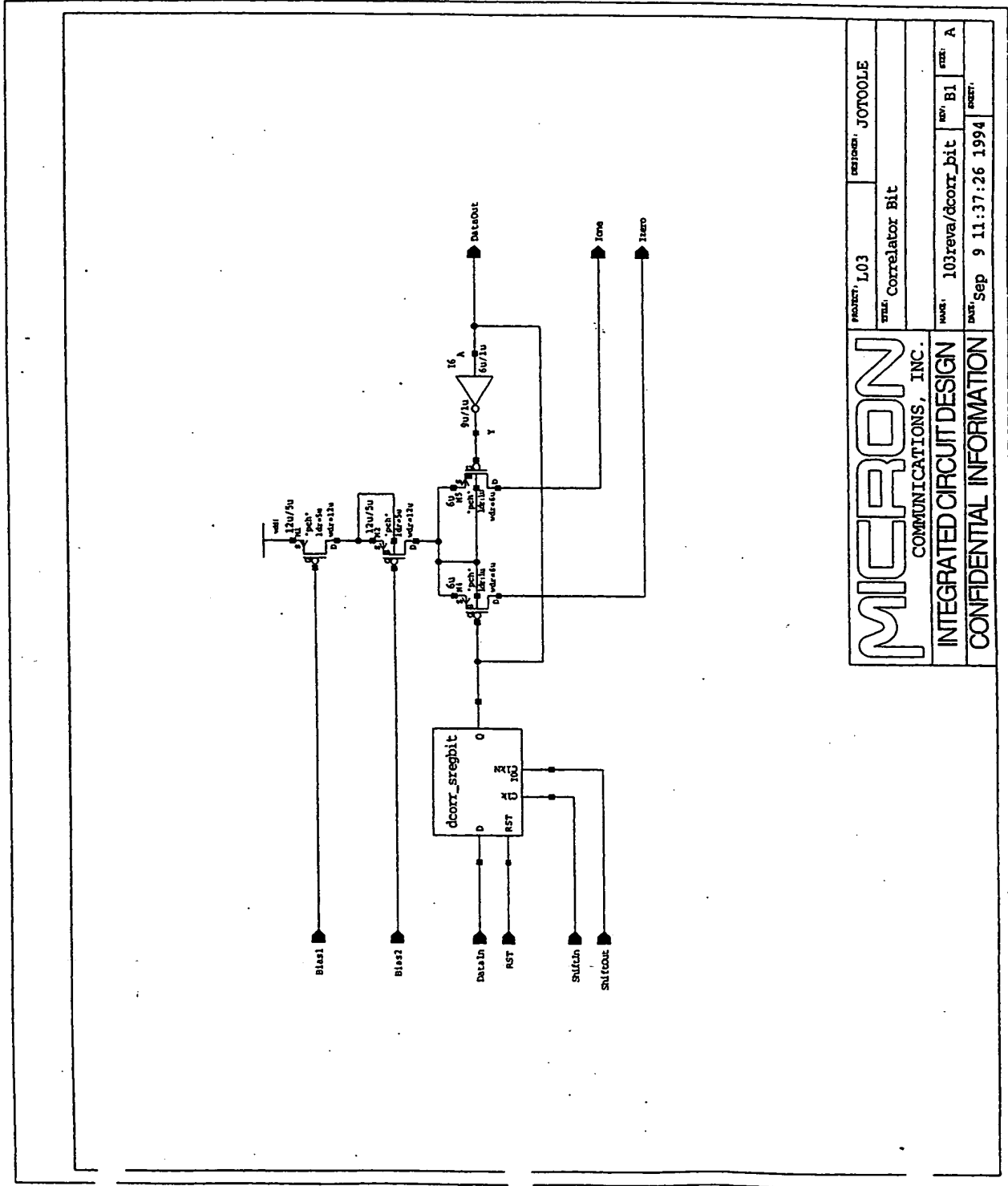


FIG. 10.010101

MICRON		PROJECT: L03	DESIGNED: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Correlator Bit	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/dcorr_bit	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 9 11:37:26 1994	SIZE: A

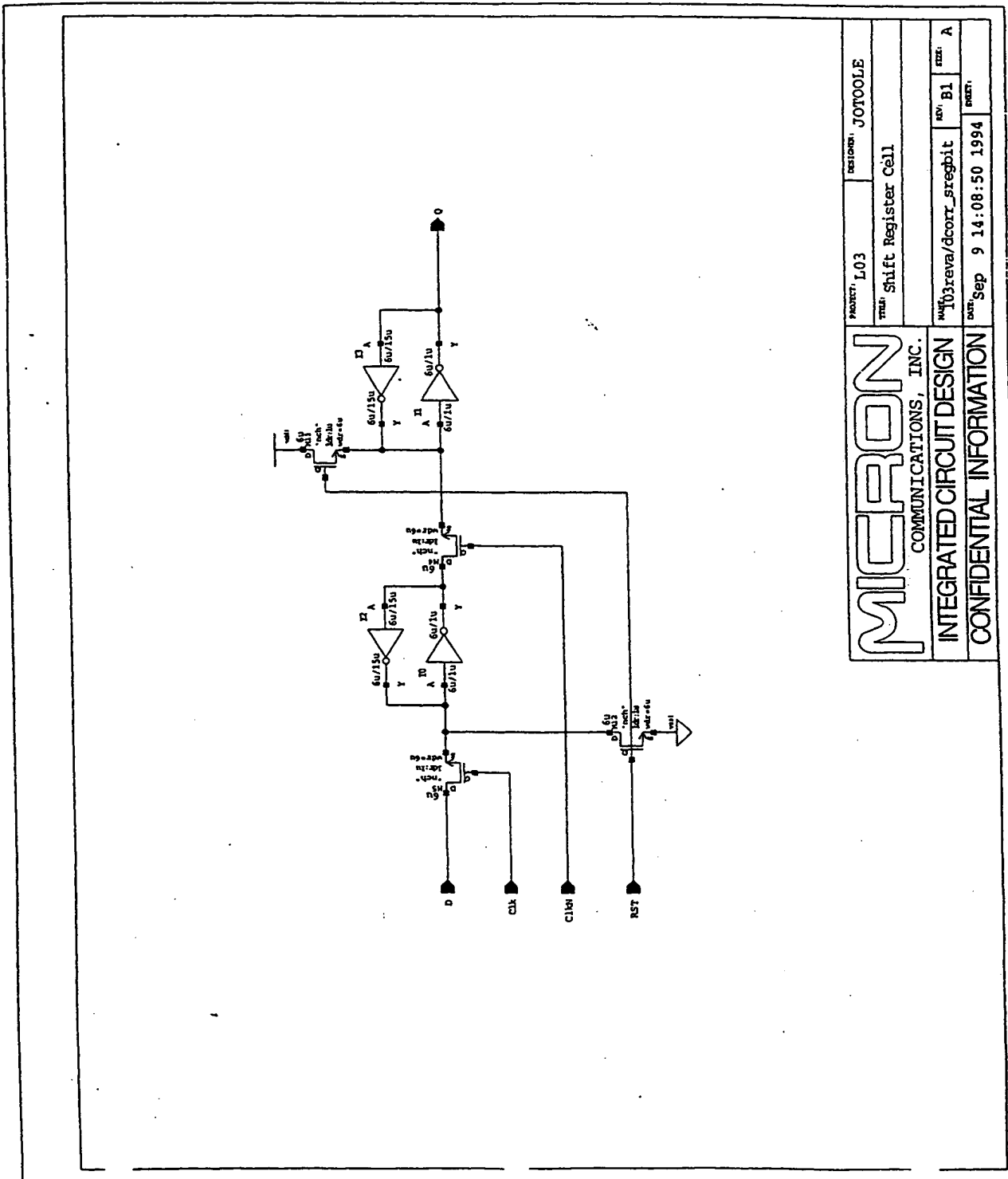


FIG. 10.01010101

MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Shift Register Cell	
INTEGRATED CIRCUIT DESIGN		NAME: T03reva/dcorr_sregbit	REV: B1
CONFIDENTIAL INFORMATION		DATE: Sep 9 14:08:50 1994	SIZE: A

10.0102AA	10.0102AB	10.0102AC	10.0102AD	10.0102AE	10.0102AF	10.0102AG	10.0102AH	10.0101AI	10.0102AJ	10.0102AK	10.0102AL	10.0102AM	10.0102AN
10.0102BA	10.0102BB	10.0102BC	10.0102BD	10.0102BE	10.0102BF	10.0102BG	10.0102BH	10.0101AI	10.0102BJ	10.0102BK	10.0102BL	10.0102BM	10.0102BN
10.0102CJ 10.0102CK 10.0102CL 10.0102CM 10.0102CN													

2001 6 2





10.02AA	10.02AB	10.02AC	10.02AD	10.02AE
10.02BA	10.02BB	10.02BC	10.02BD	10.02BE

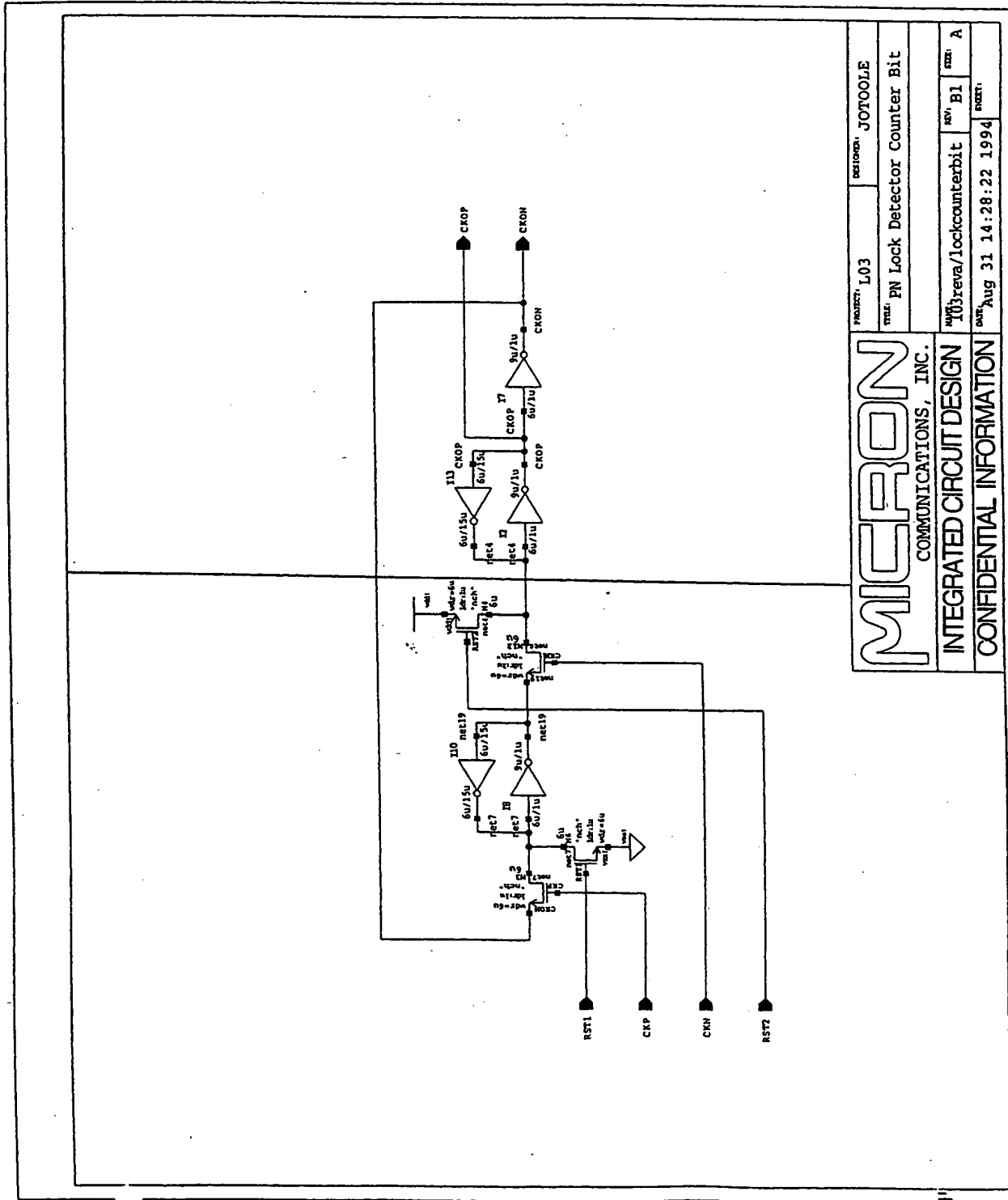
EE 10.02



10.0201AB

10.0201AA

10.0201



<b>MICRON</b>		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: PN Lock Detector Counter Bit	
INTEGRATED CIRCUIT DESIGN		REV: B1	SIZE: A
CONFIDENTIAL INFORMATION		DATE: Aug 31 14:28:22 1994	DESIGNER: JOTOOLE

FIG. 10.0201

10.03AB

10.03AA

EX-100

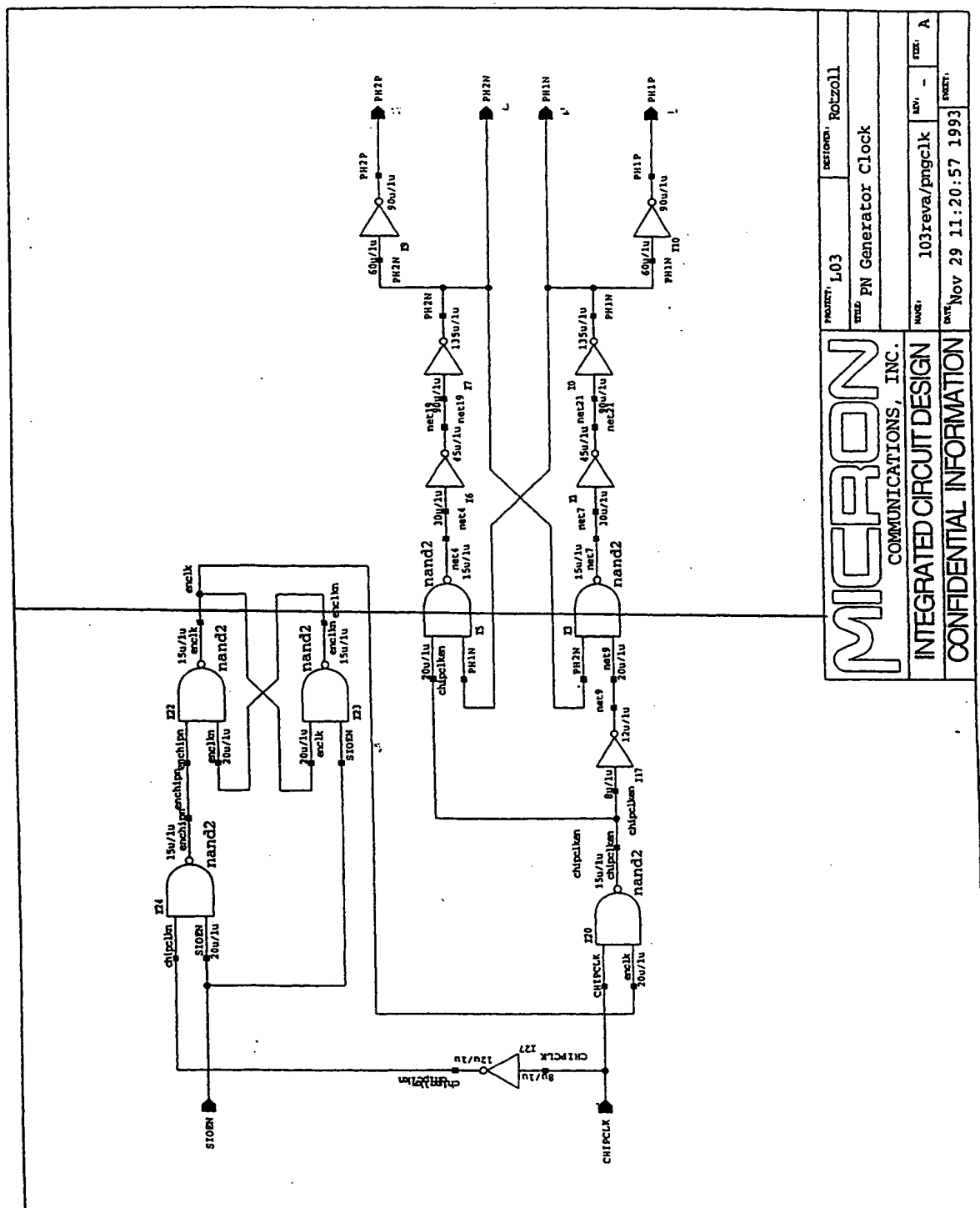


FIG. 10.03

10.04AA	10.04AB	10.04AC	10.04AD	10.04AE
10.04BA	10.04BB	10.04BC	10.04BD	10.04BE
10.04CA	10.04CB	10.04CC	10.04CD	10.04CE

II II II II II II II II

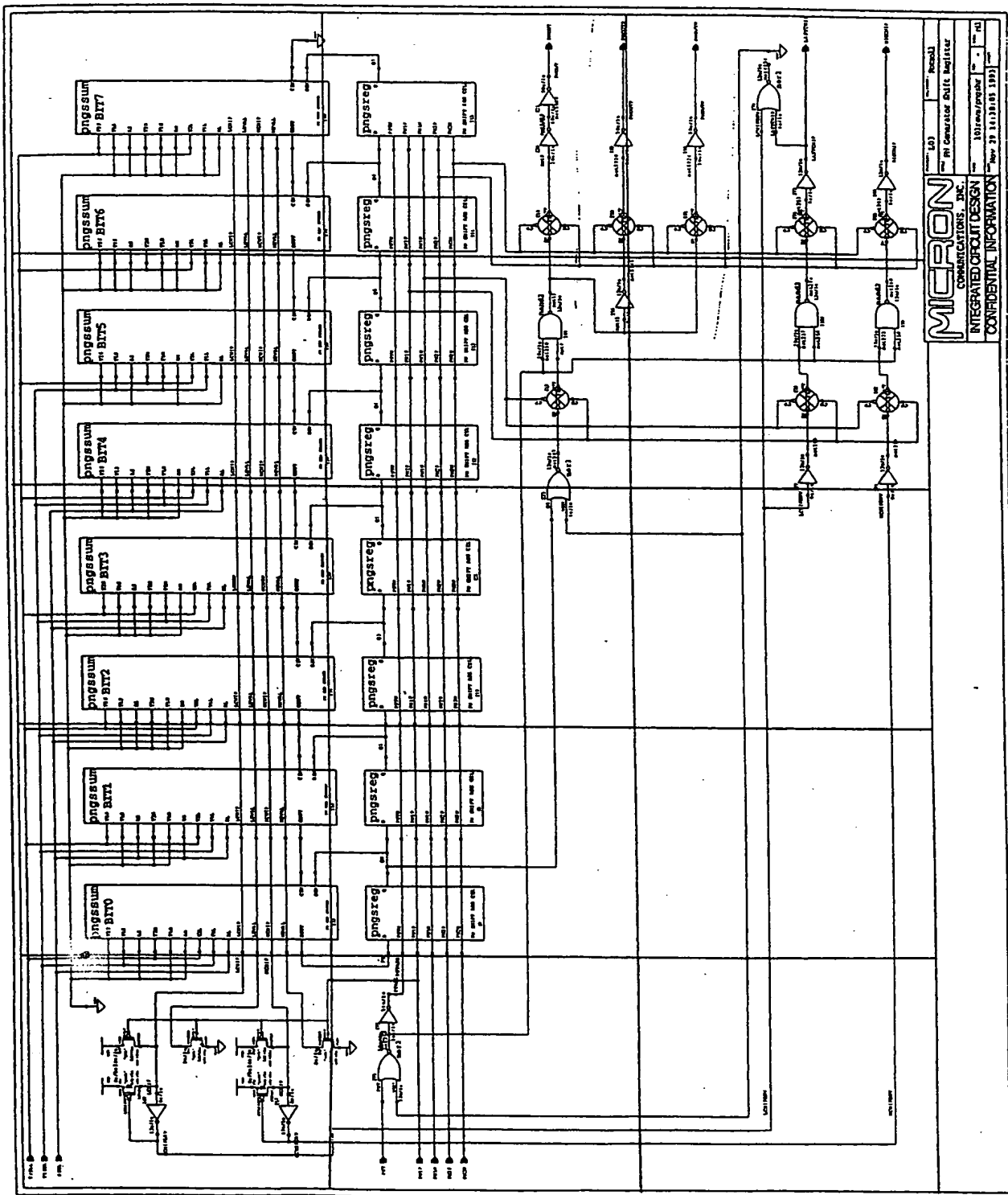


Fig. 10.04

**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION



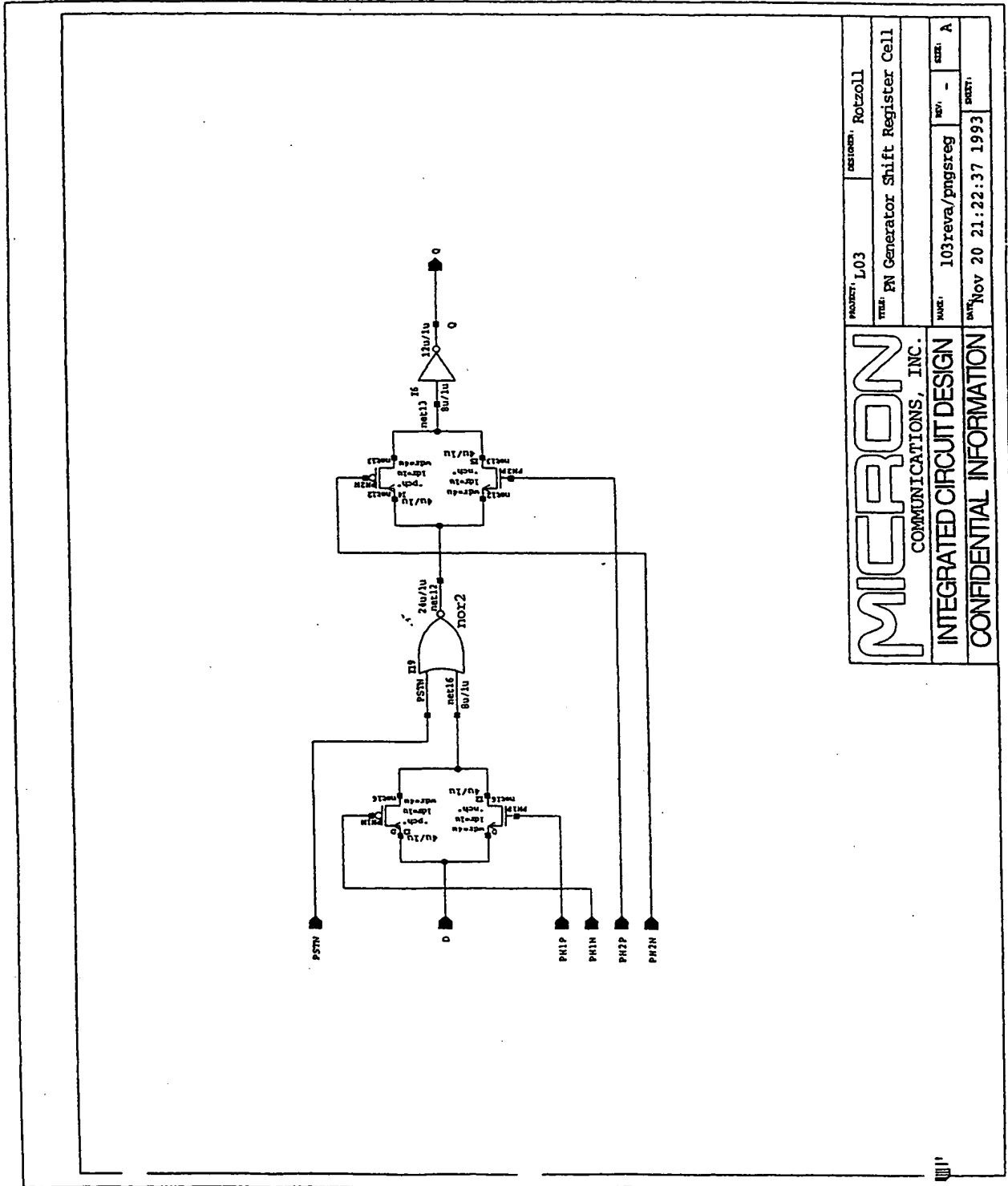


Fig. 10.0401

PROJECT: L03		DESIGNER: Rotzoll	
TITLE: PN Generator Shift Register Cell			
NAME: 103reva/pnsgreg	REV: -	SIZE: A	
DATE: Nov 20 21:22:37 1993		SHEET: 1	

10.0402AA	10.0402AB
10.0402BA	10.0402BB
10.0402CA	10.0402CB

EX-100402

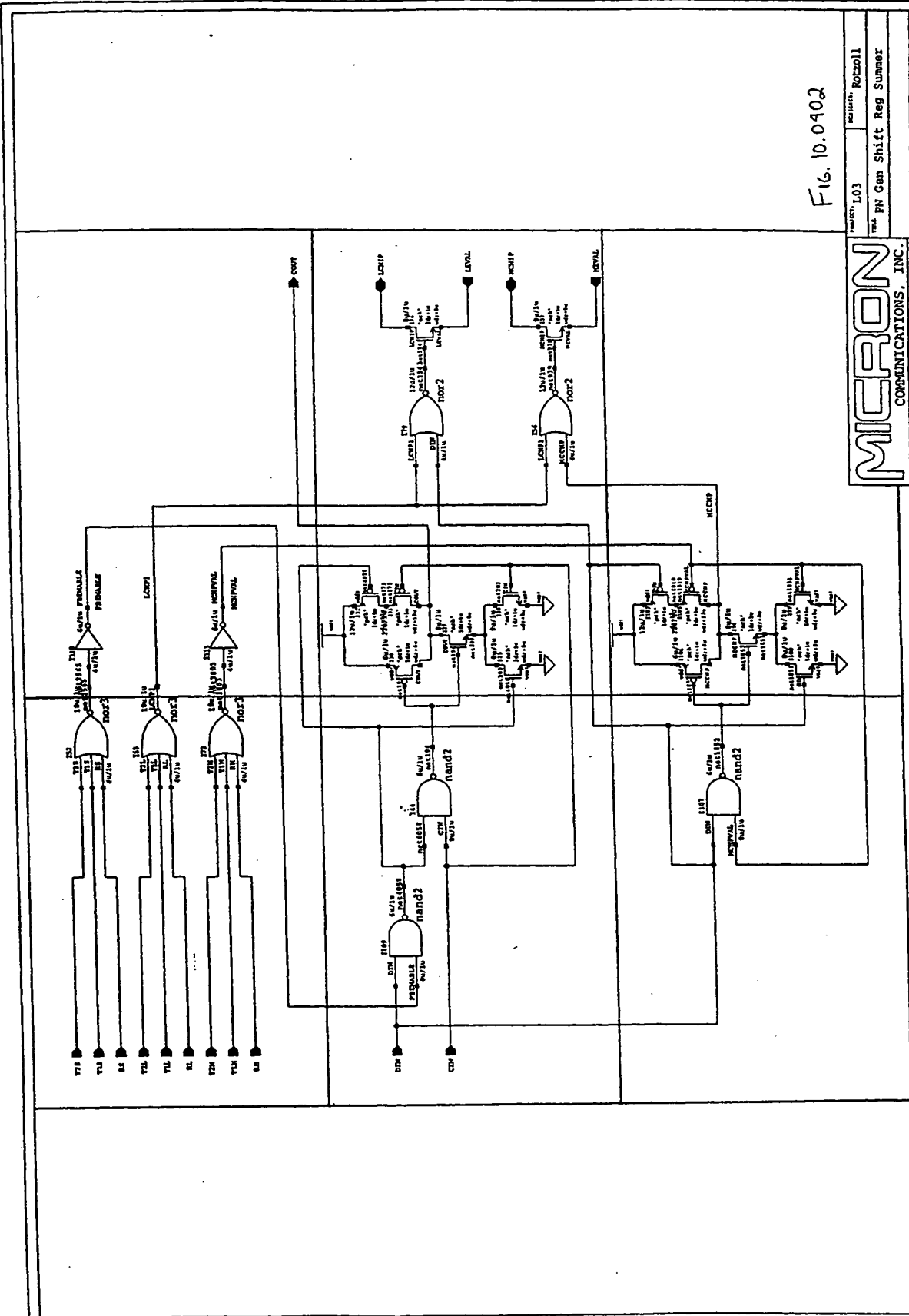
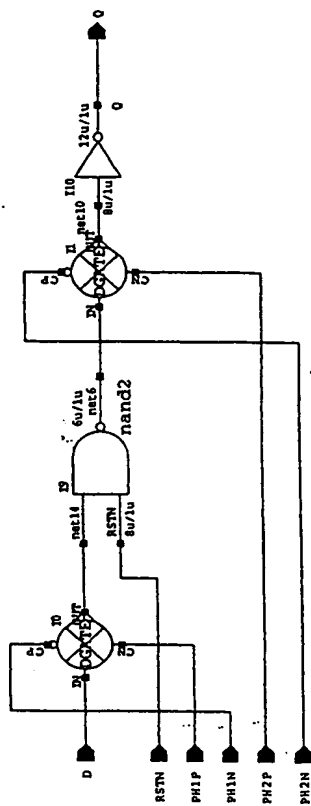


FIG. 10.0402

MICRON		PROPERTY: L03	REVISION: R020011
INTEGRATED CIRCUIT DESIGN		TITLE: PN Gen Shift Reg Summer	
CONFIDENTIAL INFORMATION		DATE: 10/26/93	BY: RLL
		DATE: Nov 20 21:23:00 1993	BY:

FIG. 10.05



PROJECT: L03		DESIGNER: Rotzoll	
TITLE: FN Controller D Flip-Flop			
NAME:	103reva/pnddfff	REV:	A
DATE:	Nov 26 18:12:59 1993	SHEET:	
MICRON COMMUNICATIONS, INC.			
INTEGRATED CIRCUIT DESIGN			
CONFIDENTIAL INFORMATION			

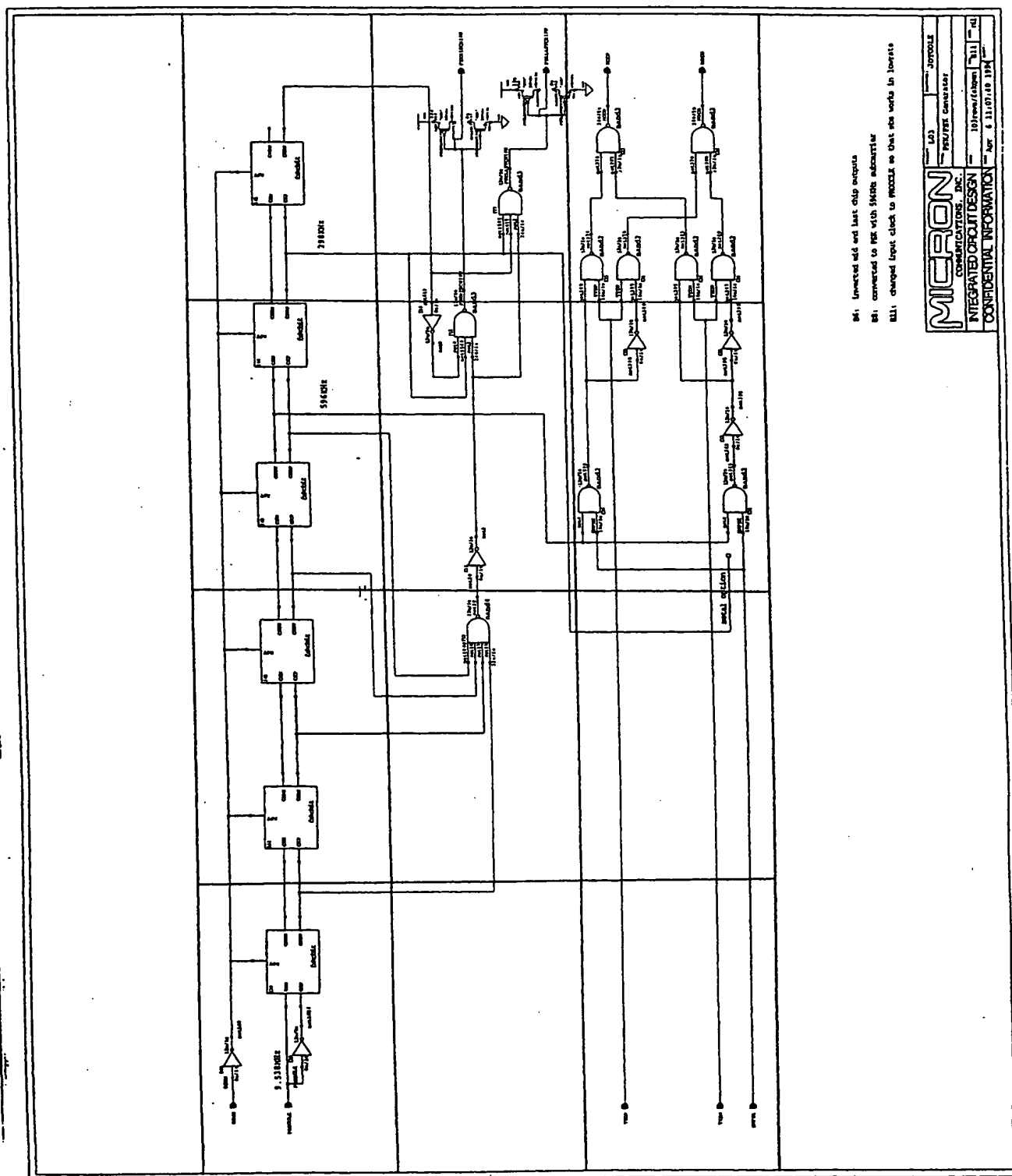
10.06AA	10.06AB	10.06AC	10.06AD								
10.06BA	10.06BB	10.06BC	10.06BD	10.06BE	10.06BF	10.06BG	10.06BH	10.06BI	10.06BJ	10.06BK	
10.06CA	10.06CB	10.06CC	10.06CD	10.06CE	10.06CF	10.06CG	10.06CH	10.06CI	10.06CJ	10.06CK	
10.06DA	10.06DB	10.06DC	10.06DD	10.06DE	10.06DF	10.06DG	10.06DH				

10.06.1988



10.07AA	10.07AB	10.07AC	10.07AD
10.07BA	10.07BB	10.07BC	10.07BD
10.07CA	10.07CB	10.07CC	10.07CD

II II II II II



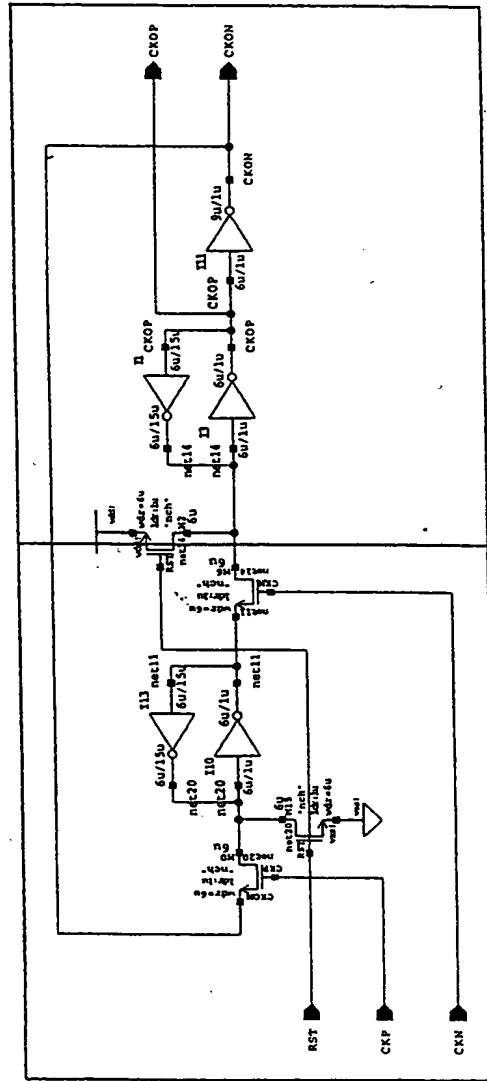


10.0701AB

10.0701AA

EX 10.0701

FIG. 10.0701

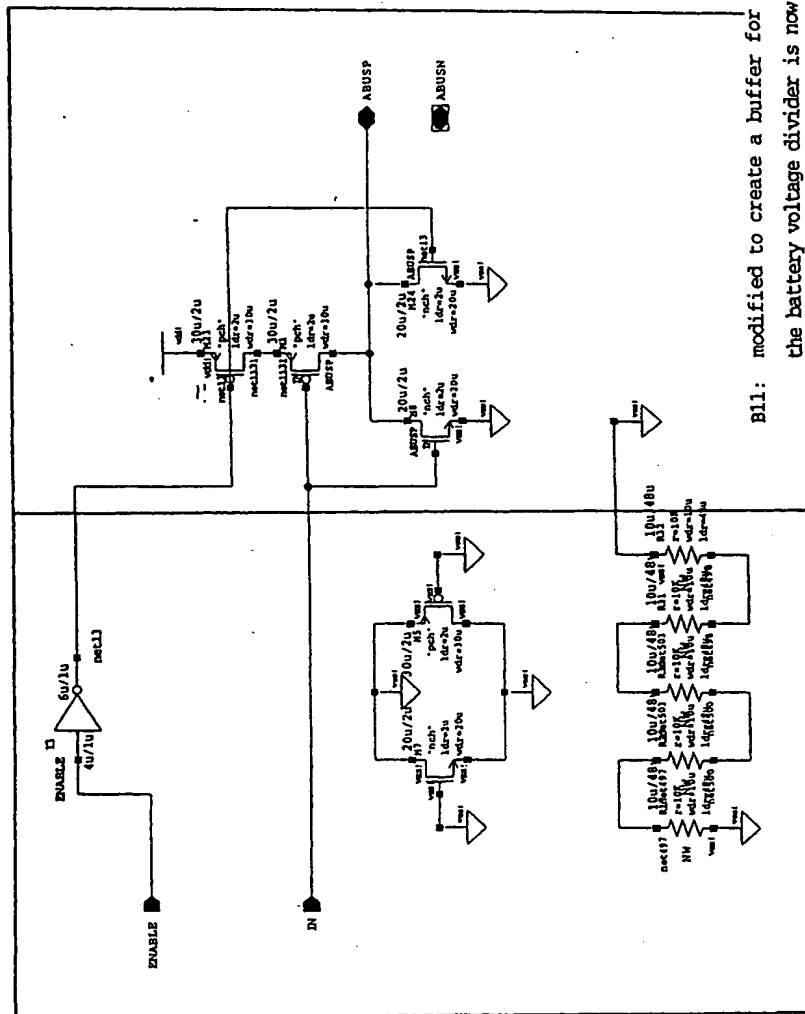


MICRON		PROPERTY	L03	DESIGNER	JOTOOLE
COMMUNICATIONS, INC.		TITLE			
INTEGRATED CIRCUIT DESIGN		FSK Counter Bit			
CONFIDENTIAL INFORMATION		Same as wuabot_cbit			
		DATE	103reva/fskcbit	REV	B1
		DATE	Apr 17 15:42:44 1995	REV	A
		PAGE			
		1			

11AA	11AB
------	------

11 11

Fig. 11



B11: modified to create a buffer for the opamp output  
the battery voltage divider is now part of tsn

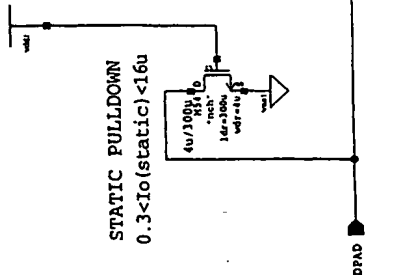
MICRON		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		NAME: Battery Analog I/O Buffer	
INTEGRATED CIRCUIT DESIGN		NO. 103reva/batalg	REV: B11
CONFIDENTIAL INFORMATION		DATE: Apr 8 10:19:56 1996	SHEET: A

12AB

12AA

112





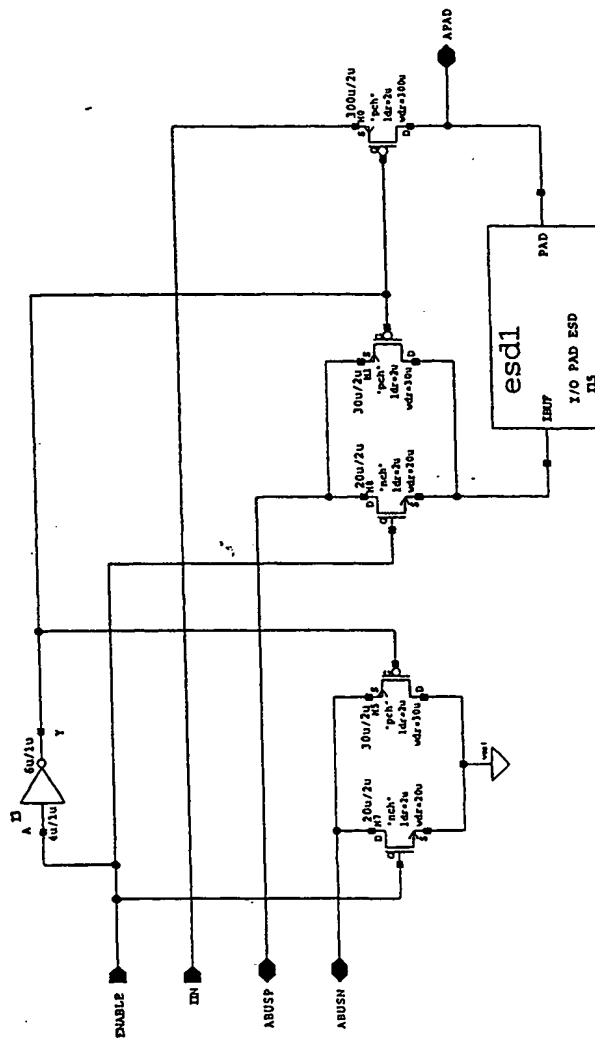
STATIC PULLDOWN  
 $0.3 < I_o(\text{static}) < 16\mu$

<b>MICRON</b>		PROJECT: L03	DESIGNER: JOTOOLE
COMMUNICATIONS, INC.		TITLE: Digital Input Pad Buffer	
INTEGRATED CIRCUIT DESIGN		NAME: 103reva/paddigin	REV: B1
CONFIDENTIAL INFORMATION		DATE: Apr 11 11:10:35 1995	DES: A

FIG. 13







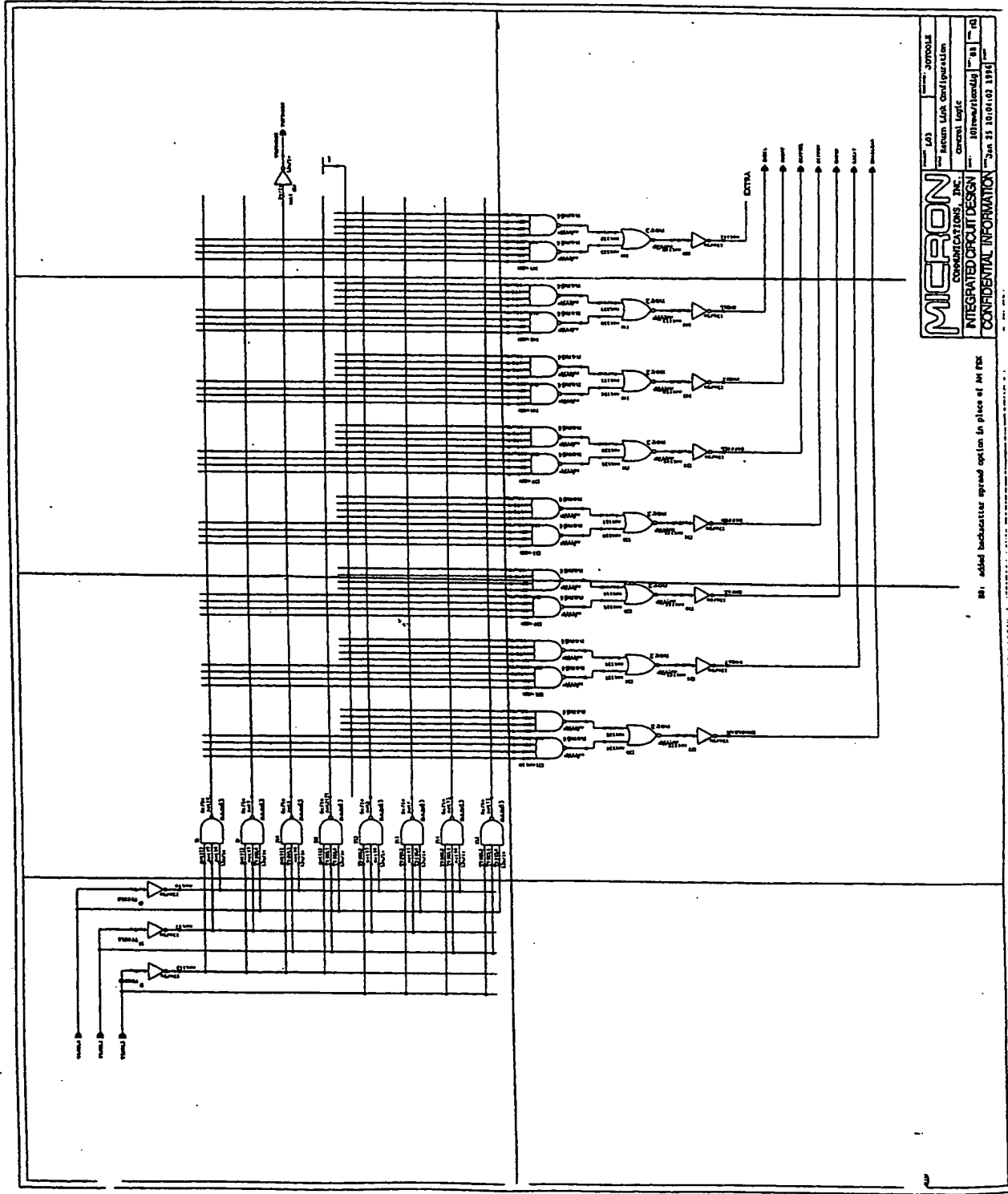
<b>MICRON</b>		DESIGNER: Rotzoll
COMMUNICATIONS, INC.		PRODUCT: L03
INTEGRATED CIRCUIT DESIGN		TITLE: Analog I/O Pad Buffer
CONFIDENTIAL INFORMATION		NAME: 103reva/padalg
		REV: -
		DATE: Dec 12 21:55:41 1993
		SHEET: A

FIG. 19

15AA	15AB	15AC	15AD	15BA	15BB	15BC
------	------	------	------	------	------	------

EX-15

FIG. 15



**MICRON**  
COMMUNICATIONS, INC.  
INTEGRATED CIRCUIT DESIGN  
CONFIDENTIAL INFORMATION

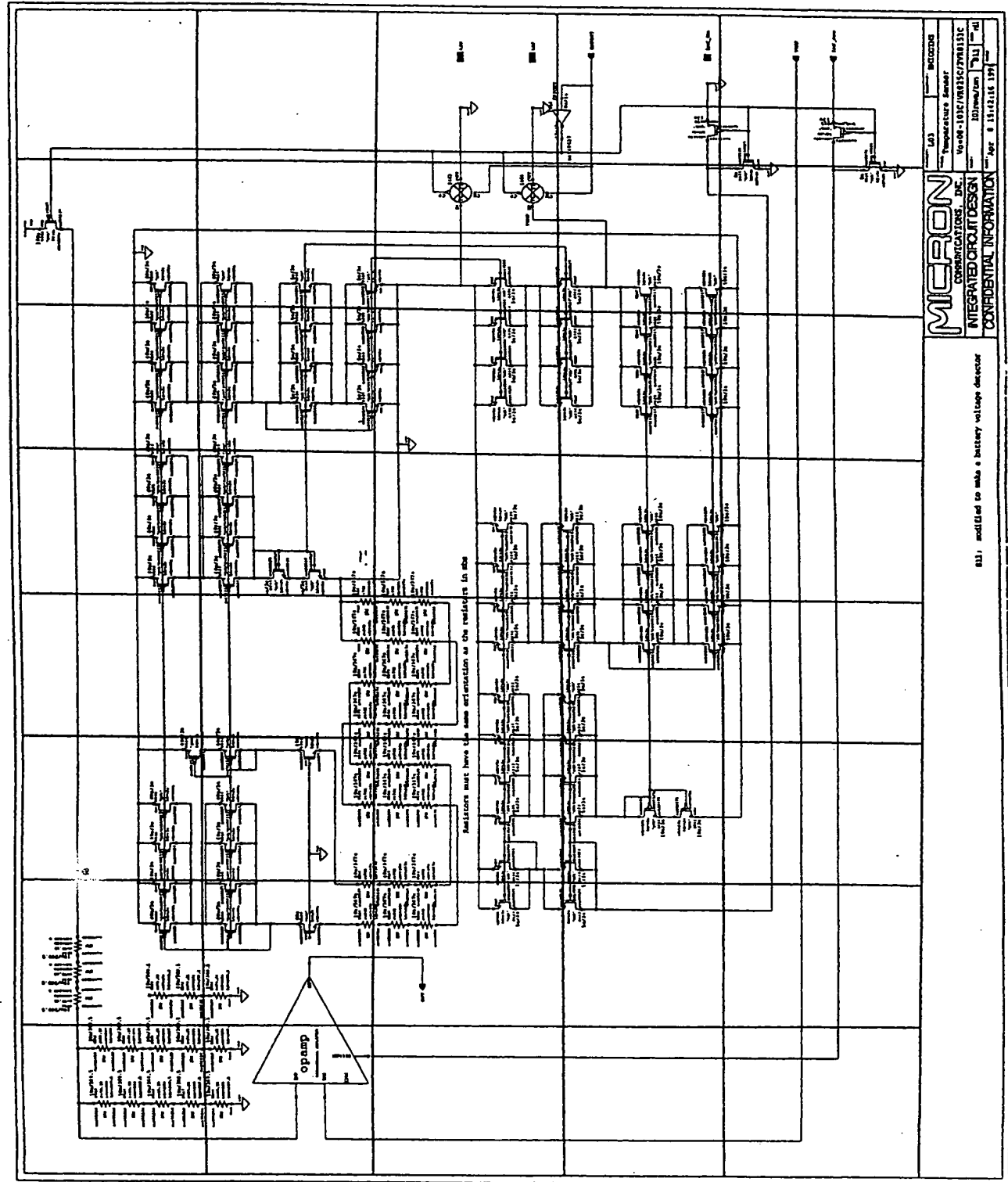
801 added backscatter spread option in place of 801 PSC

DATE: 10/01/03  
DESIGNER: J. J. JORDAN  
CHECKED: J. J. JORDAN  
APPROVED: J. J. JORDAN

16AA	16AB	16AC	16AD	16AE	16AF	16AG	16AH
16BA	16BB	16BC	16BD	16BE	16BF	16BG	16BH
16CA	16CB	16CC	16CD	16CE	16CF	16CG	16CH
16DA	16DB	16DC	16DD	16DE	16DF	16DG	16DH
16EA	16EB	16EC	16ED	16EE	16EF	16EG	16EH

IL 11 11 11

Fig. 16

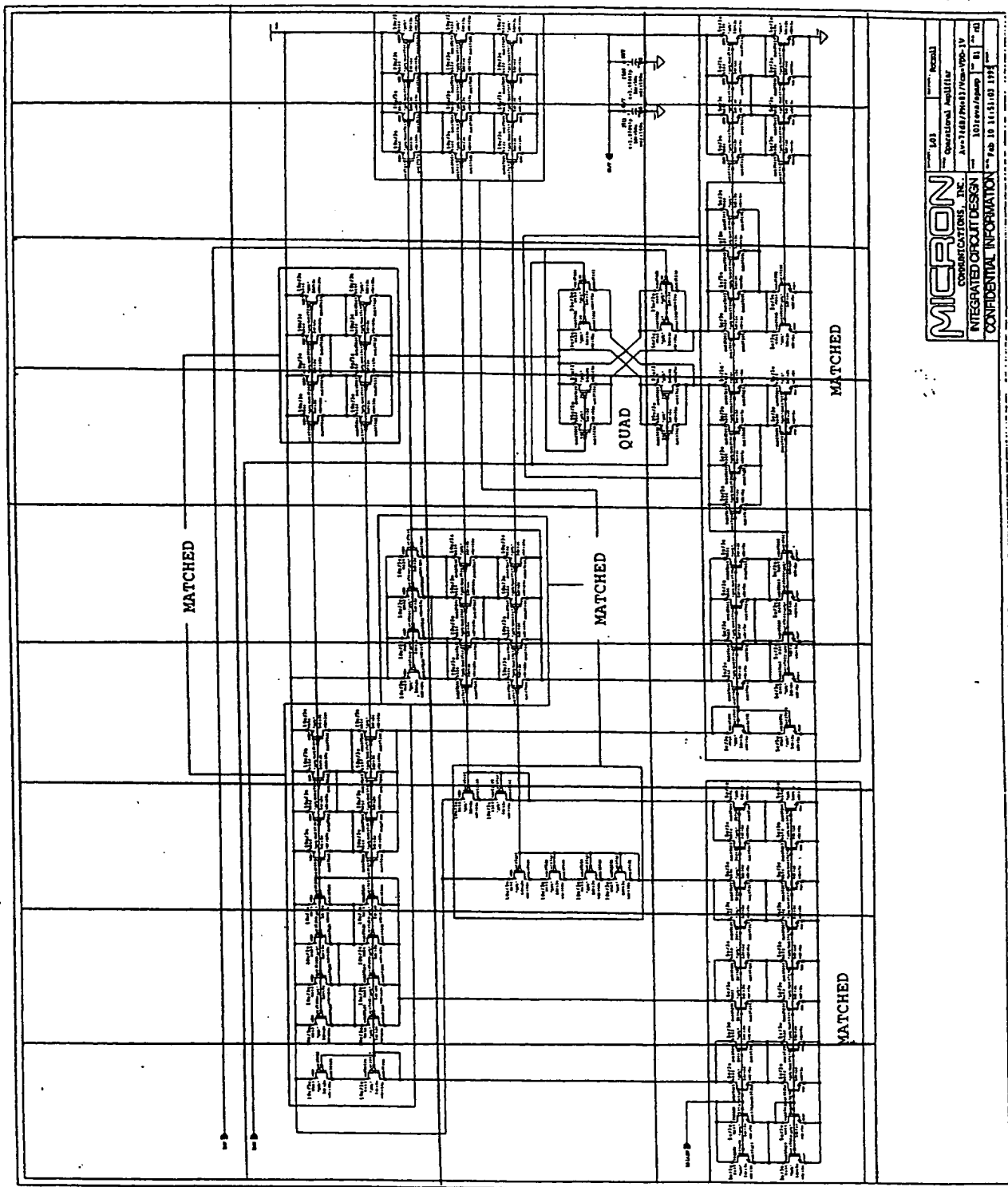


80000 modified to make a battery voltage detector

16.01AA	16.01AB	16.01AC	16.01AD	16.01AE	16.01AF	16.01AG		
16.01BA	16.01BB	16.01BC	16.01BD	16.01BE	16.01BF	16.01BG	16.01BH	16.01BI
16.01CA	16.01CB	16.01CC	16.01CD	16.01CE	16.01CF	16.01CG	16.01CH	16.01CI
16.01DA	16.01DB	16.01DC	16.01DD	16.01DE	16.01DF	16.01DG	16.01DH	16.01DI

II II II II II II II II II

FIG. 16.01



<b>MICRON</b>		Part	Rev
MICRON TECHNOLOGIES, INC.		Operational Amplifier	
INTEGRATED CIRCUIT DESIGN		Amplifier/Comparator	10
CONFIDENTIAL INFORMATION		101rev/comp	B
		Feb 18 11:51:03 1974	

17AB	17BB
17AA	17BA

EX 17





**B8: fixed control logic**

18AB	18AA
------	------

18AB

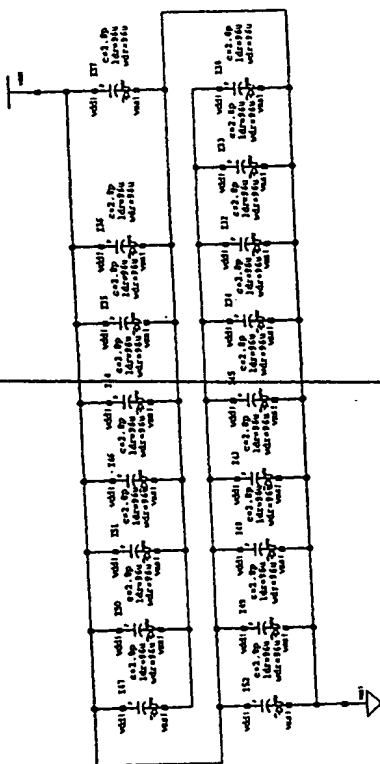


FIG. 18

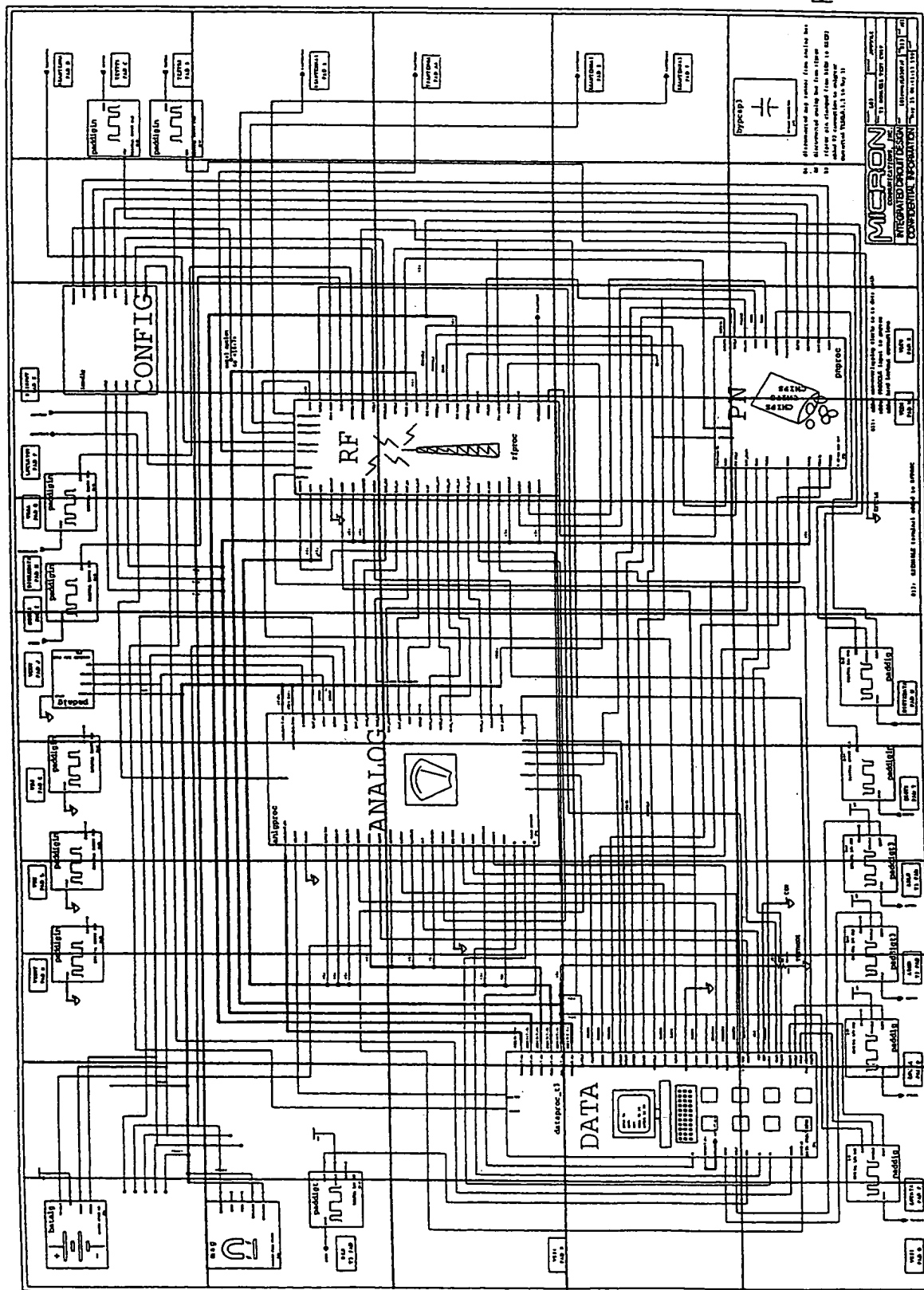
MICRON		PRODUCT: J07000LE
COMMUNICATIONS, INC.		ITEM: Chip Bypass Capacitor
INTEGRATED CIRCUIT DESIGN		CT: 103pva/bypcap3
CONFIDENTIAL INFORMATION		DATE: Jul 28 17:43:25 1995

B2: deleted one cap

19AA	19AB	19AC	19AD	19AE	19AF	19AG	19AH	19AI	19AJ	19AK
19BA	19BB	19BC	19BD	19BE	19BF	19BG	19BH	19BI	19BJ	19BK
19CA	19CB	19CC	19CD	19CE	19CF	19CG	19CH	19CI	19CJ	19CK
19DA	19DB	19DC	19DD	19DE	19DF	19DG	19DH	19DI	19DJ	19DK
19EA	19EB	19EC	19ED	19EE	19EF	19EG	19EH	19EI	19EJ	19EK

IL 11 11 11

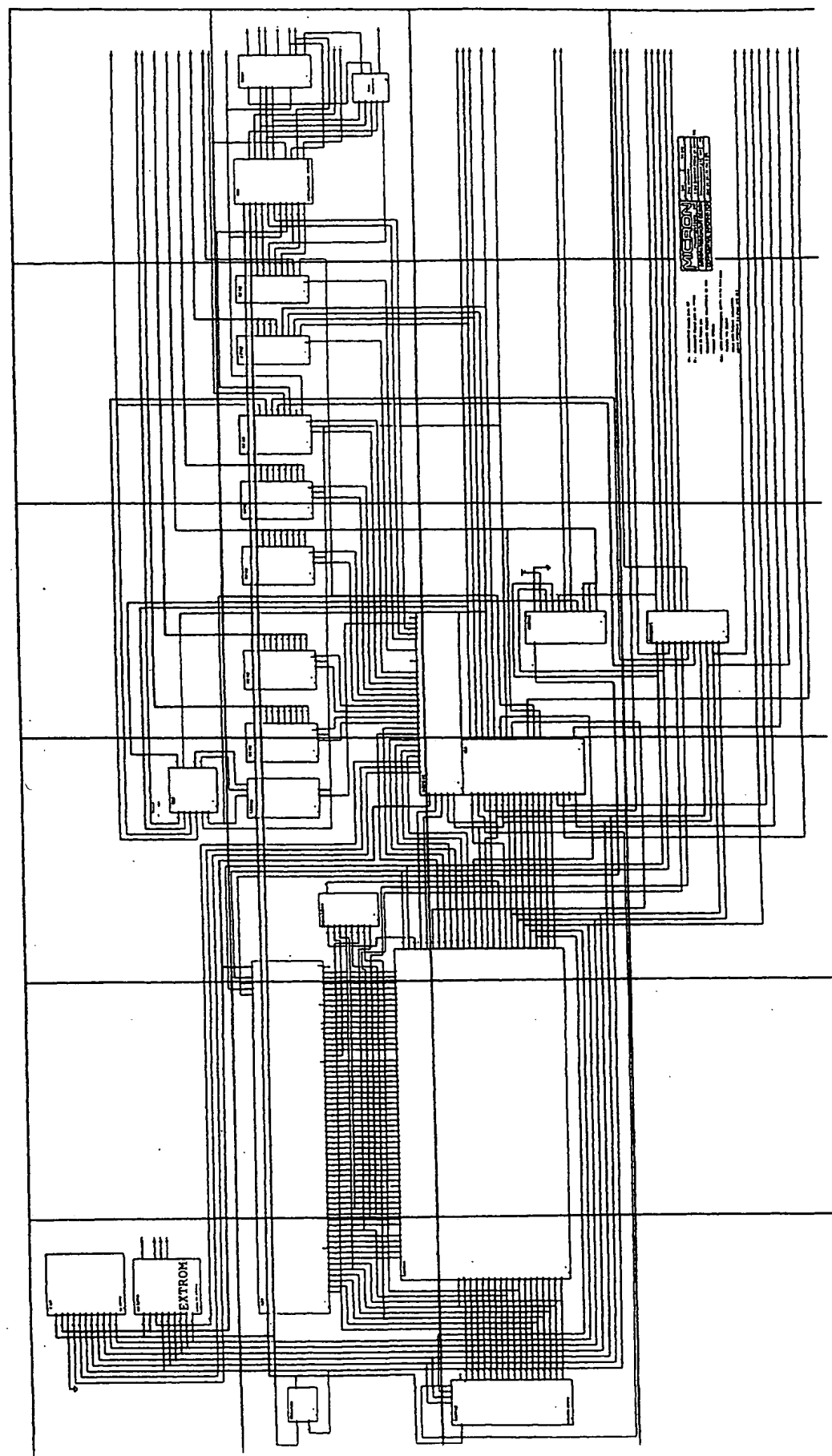
Fig. 19.AA-EK



20AA	20AB	20AC	20AD	20AE	20AF
20BA	20BB	20BC	20BD	20BE	20BF
20CA	20CB	20CC	20CD	20CE	20CF
		20DC	20DD	20DE	20DF

EX-20

FIG. 20

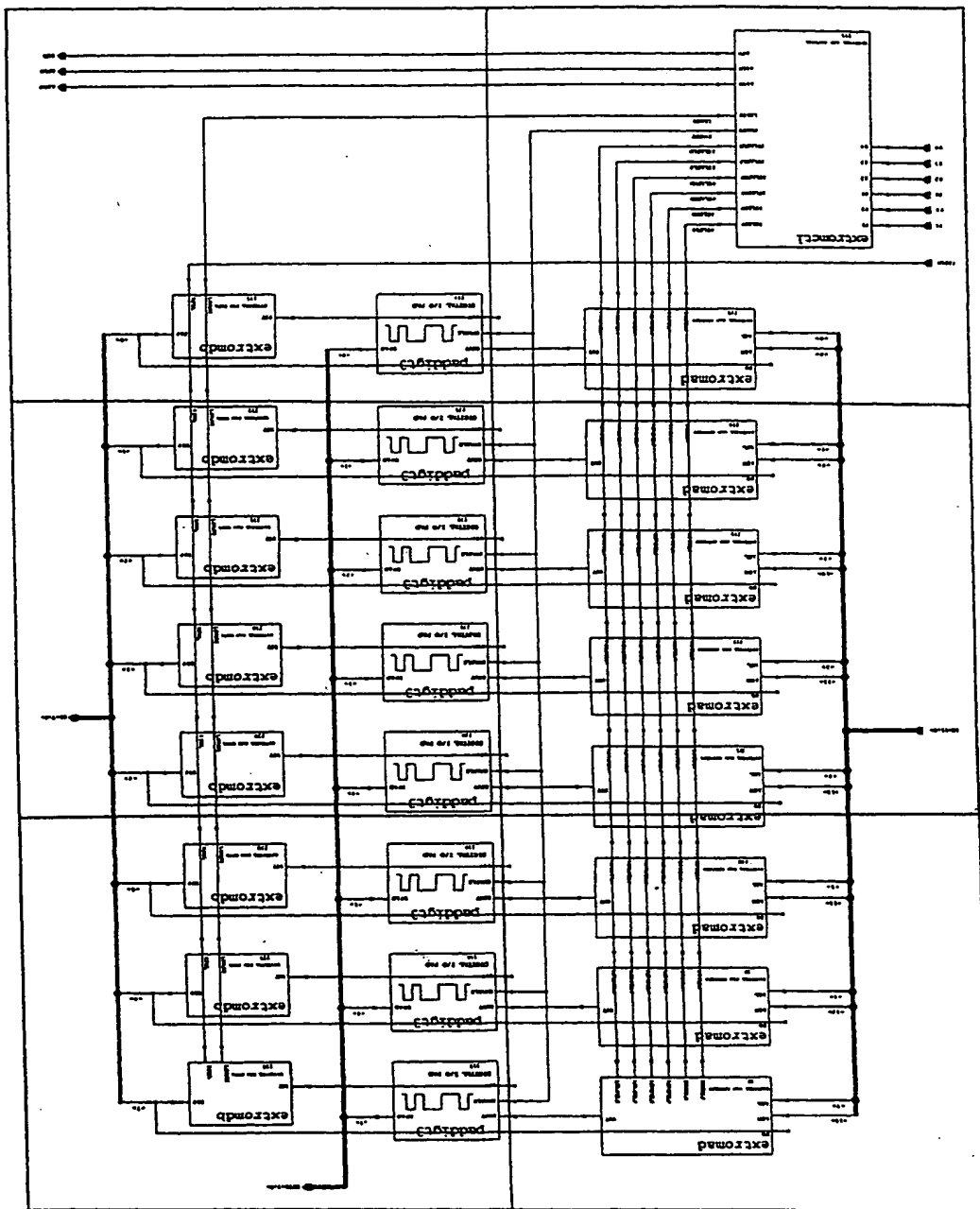


20.01AA	20.01AB
20.01BA	20.01BB
20.01CA	20.01CB

Fig 20.01



Fig. 20.01





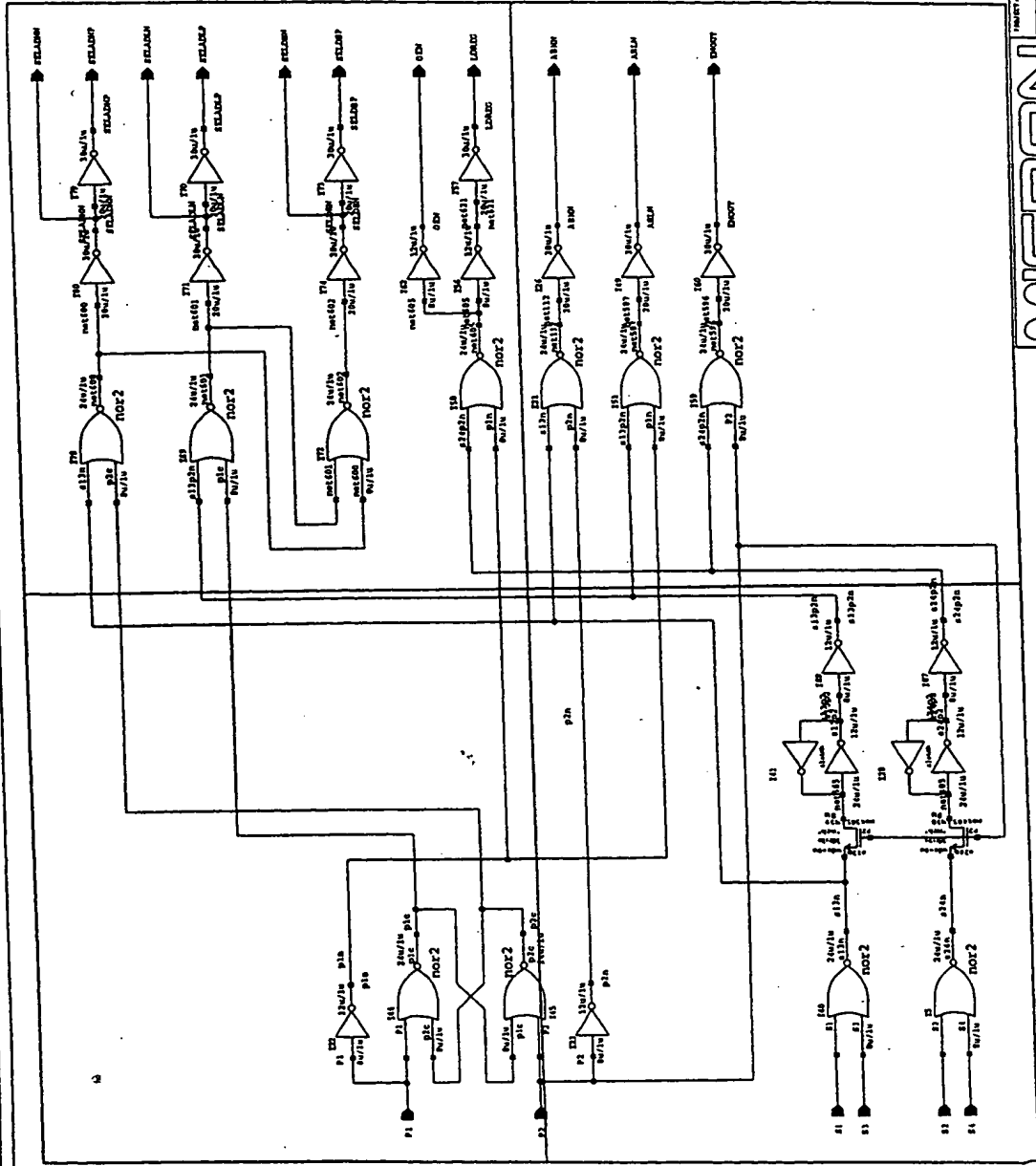
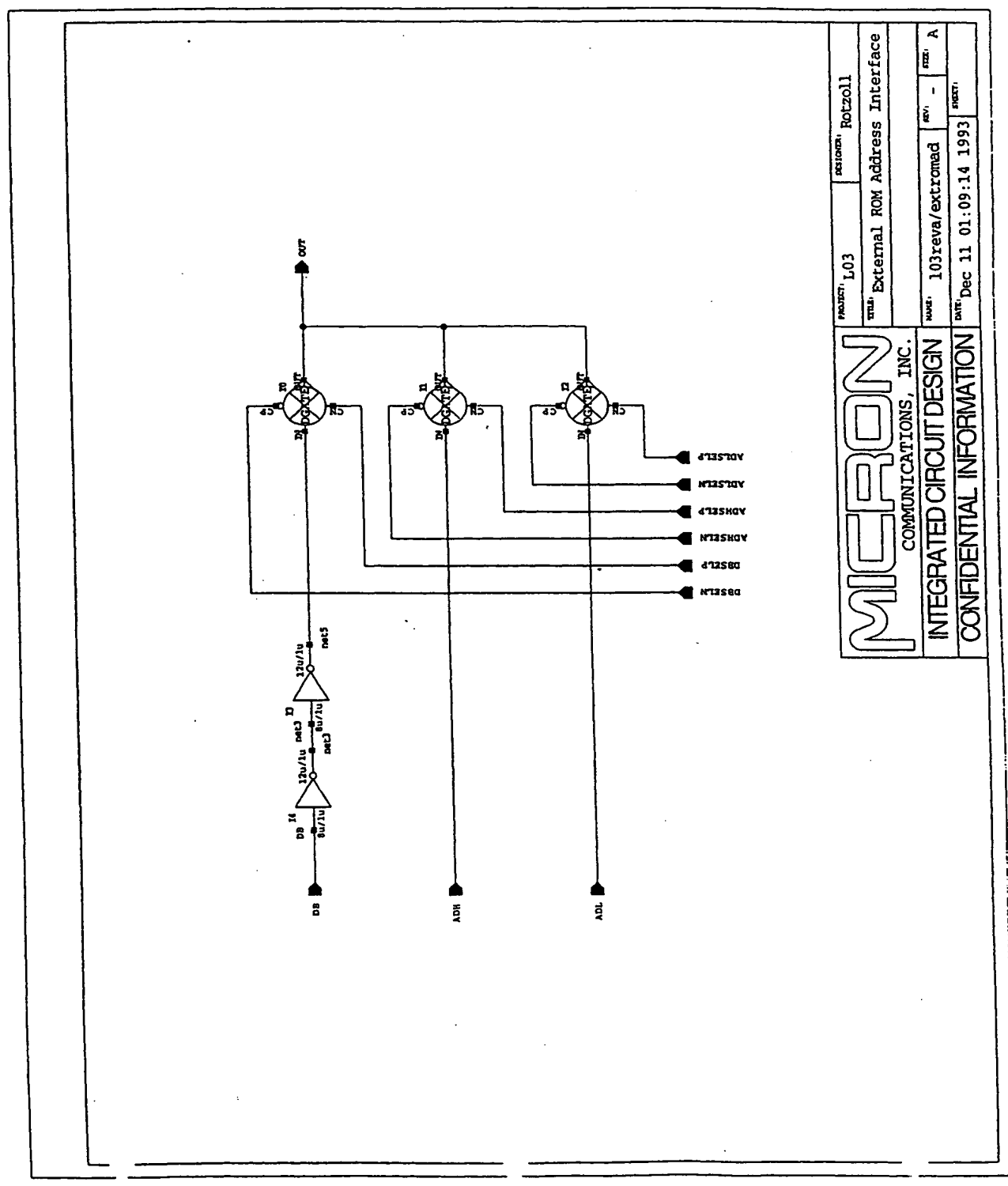


FIG. 20.0101

MICRON		MARKET	L03	REVISED	Rev 011
COMMUNICATIONS, INC.		External ROM Control Logic			
INTEGRATED CIRCUIT DESIGN		DATE	10/20/84	EXTENDED	REV - 011
CONFIDENTIAL INFORMATION		DATE	Dec 11 21:56:41 1993	REV	011

Fig. 20.0102



MICRON		DESIGNER: Rotzoll	
COMMUNICATIONS, INC.		PROJECT: L03	
INTEGRATED CIRCUIT DESIGN		TITLE: External ROM Address Interface	
CONFIDENTIAL INFORMATION		NAME: 103reva/extromad	
		REV: -	
		REV: A	
		DATE: Dec 11 01:09:14 1993	
		SHEET: 1	

**MICRON**  
 COMMUNICATIONS, INC.  
 INTEGRATED CIRCUIT DESIGN  
 CONFIDENTIAL INFORMATION

20.0103AA	20.0103AB	20.0103AC
-----------	-----------	-----------

EX 20.0103

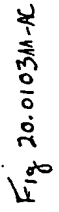
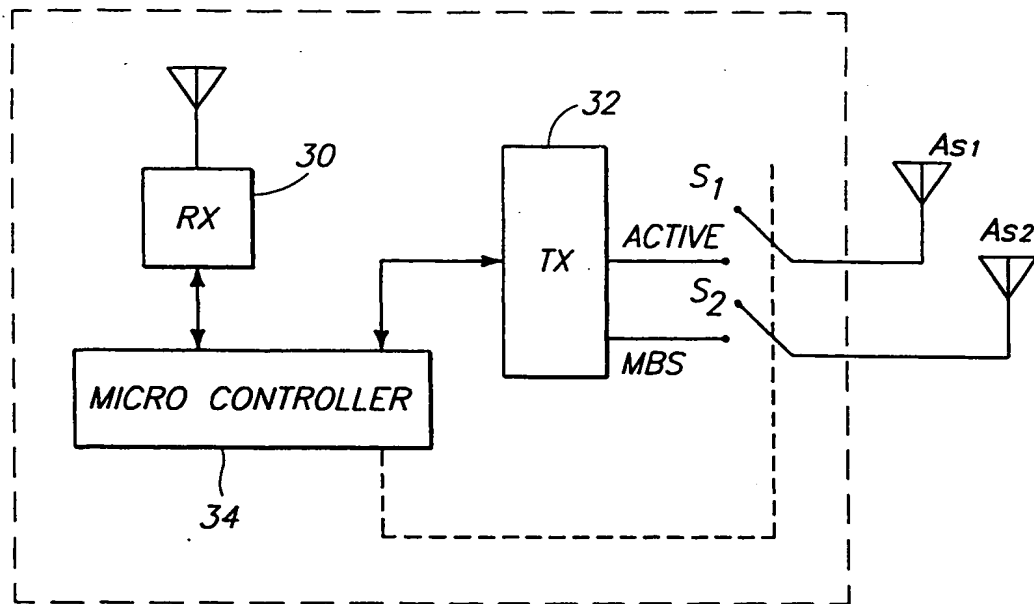
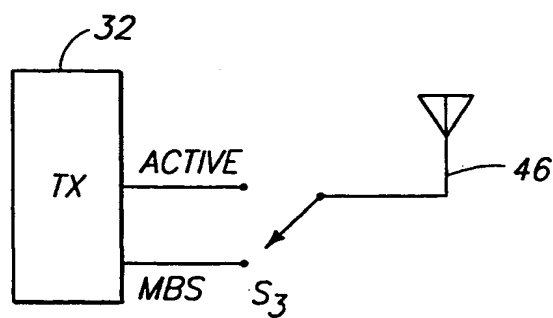
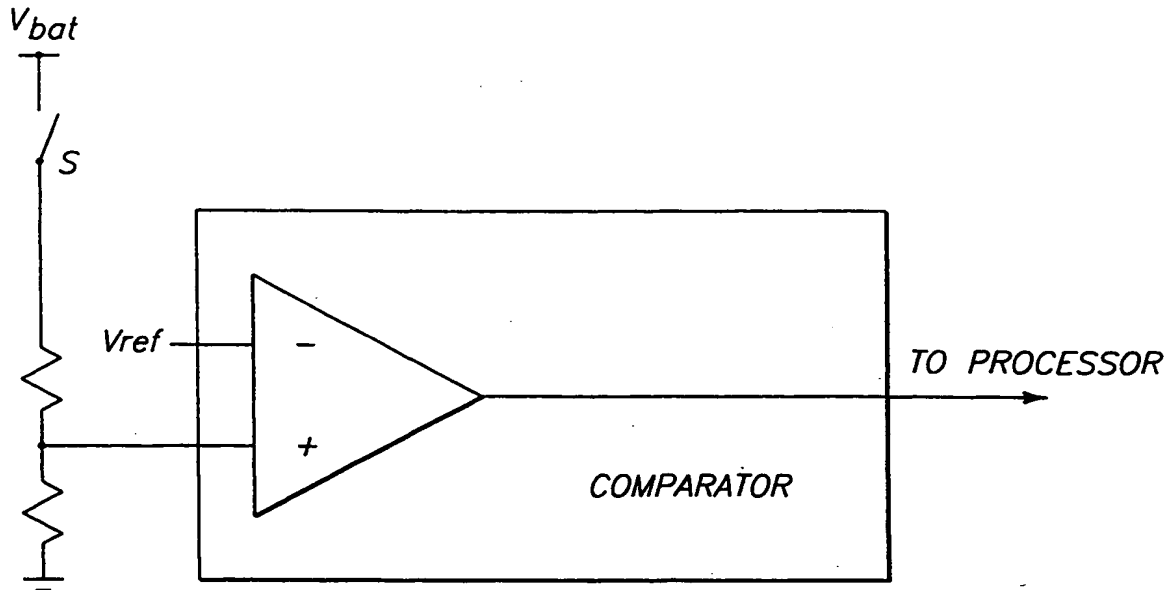


Fig 20.0103M-AC

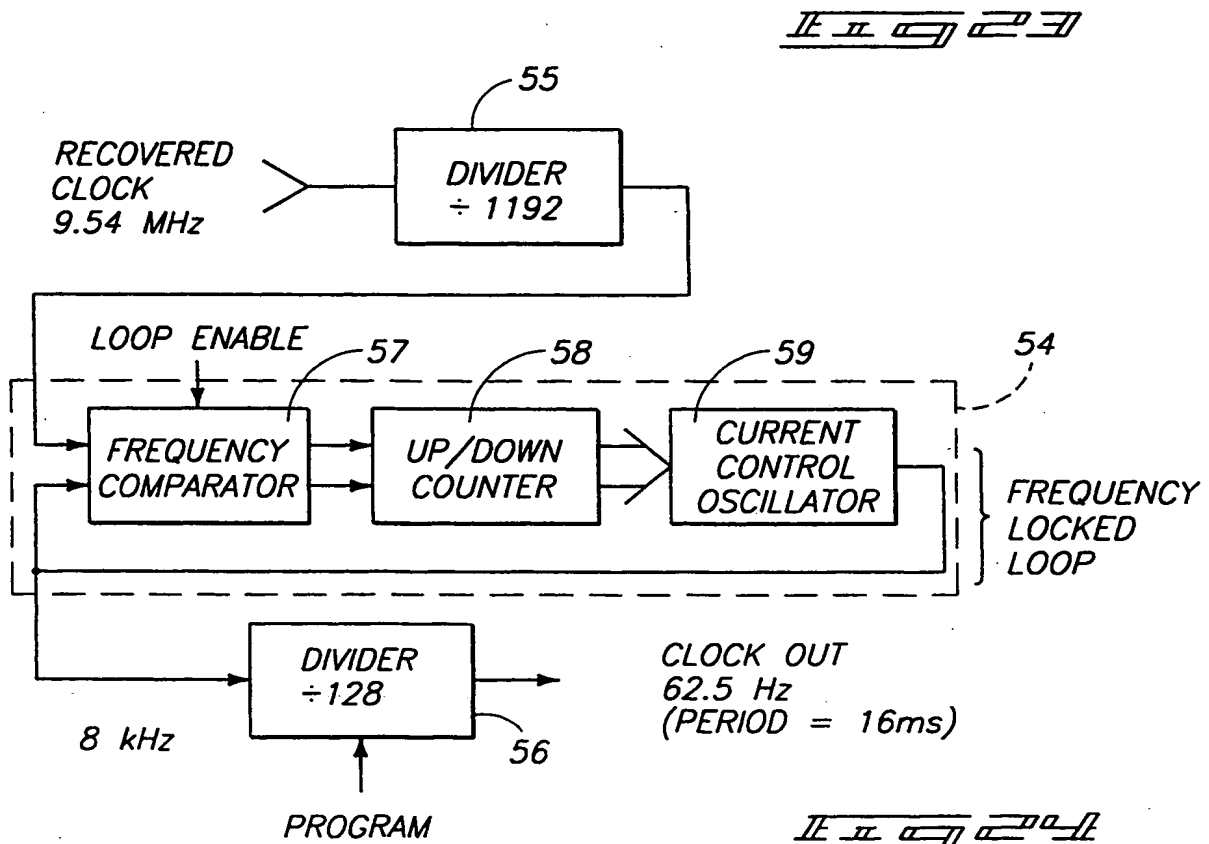


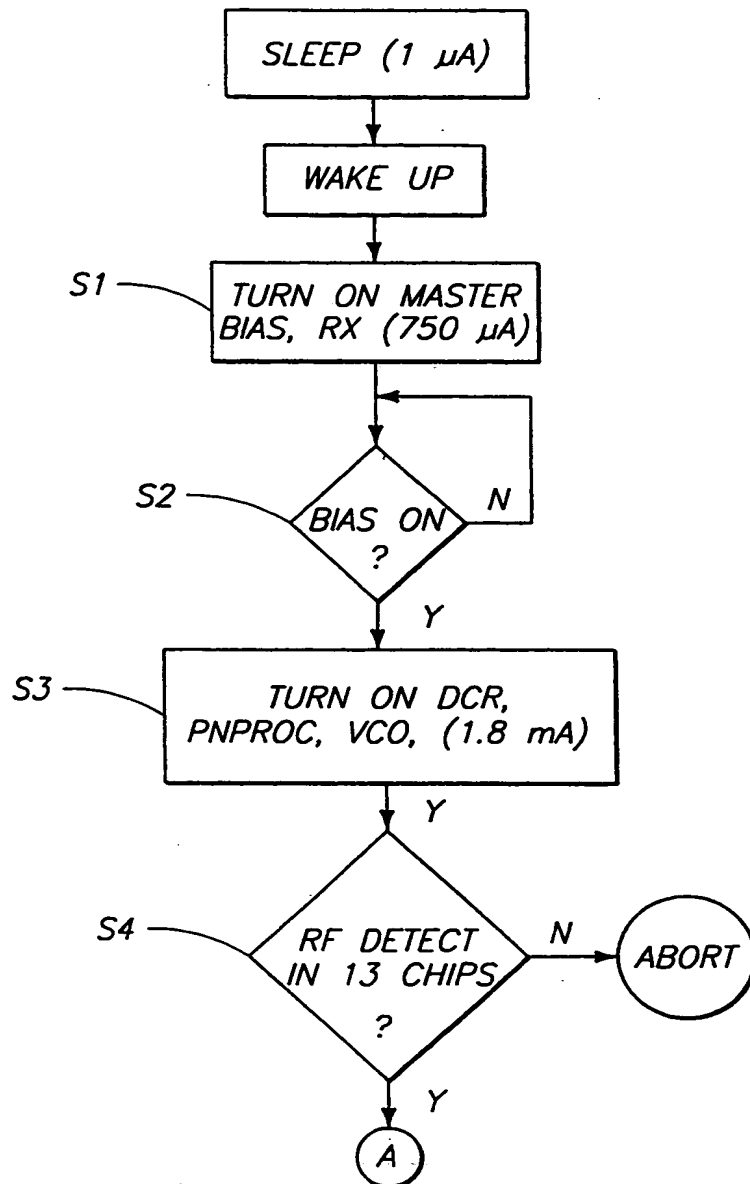
FIG. 2FIG. 3

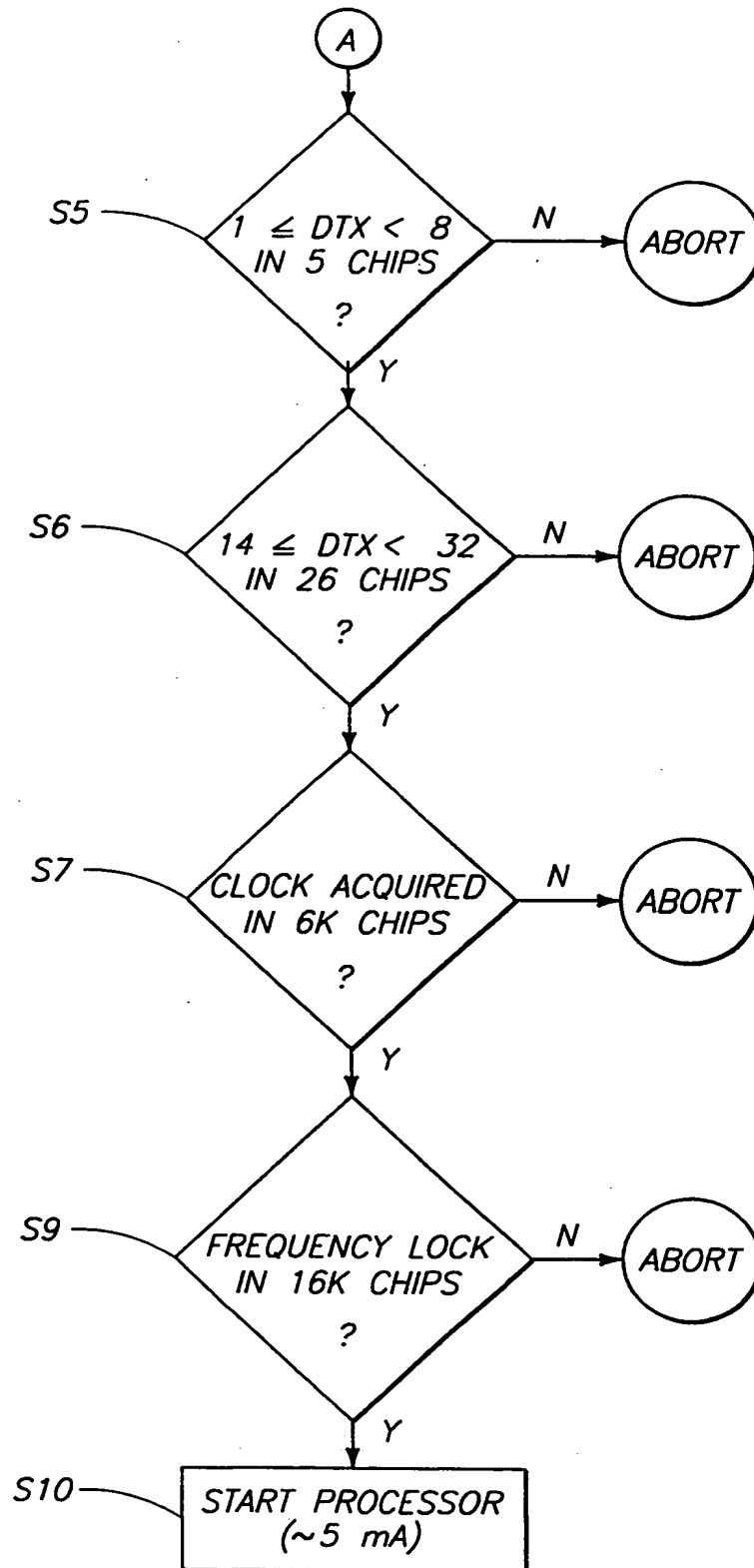


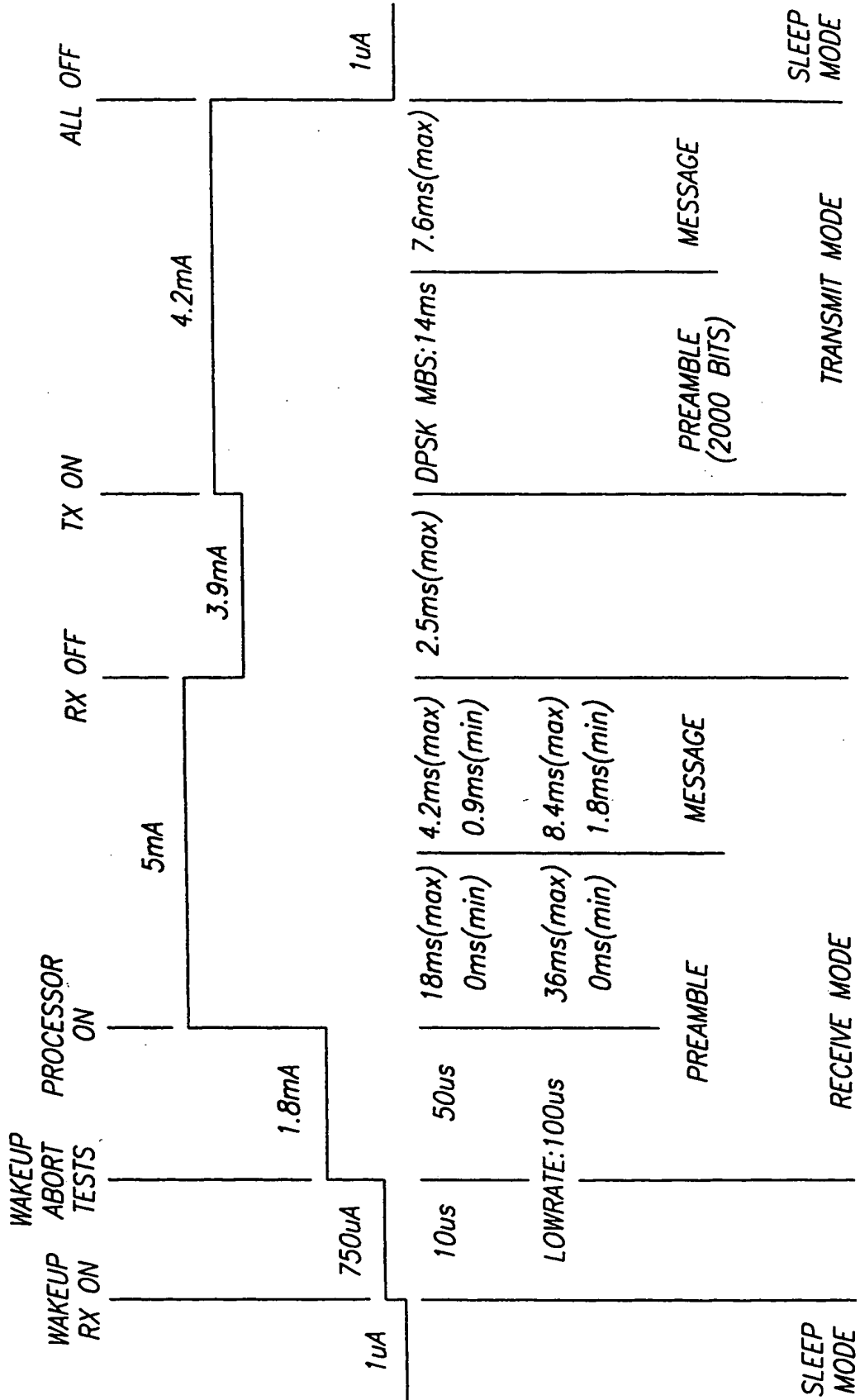


$V_{ref}$  = bandgap voltage  $\approx 1.2$  V for silicon



WAKEUP SEQUENCE





II 9 27

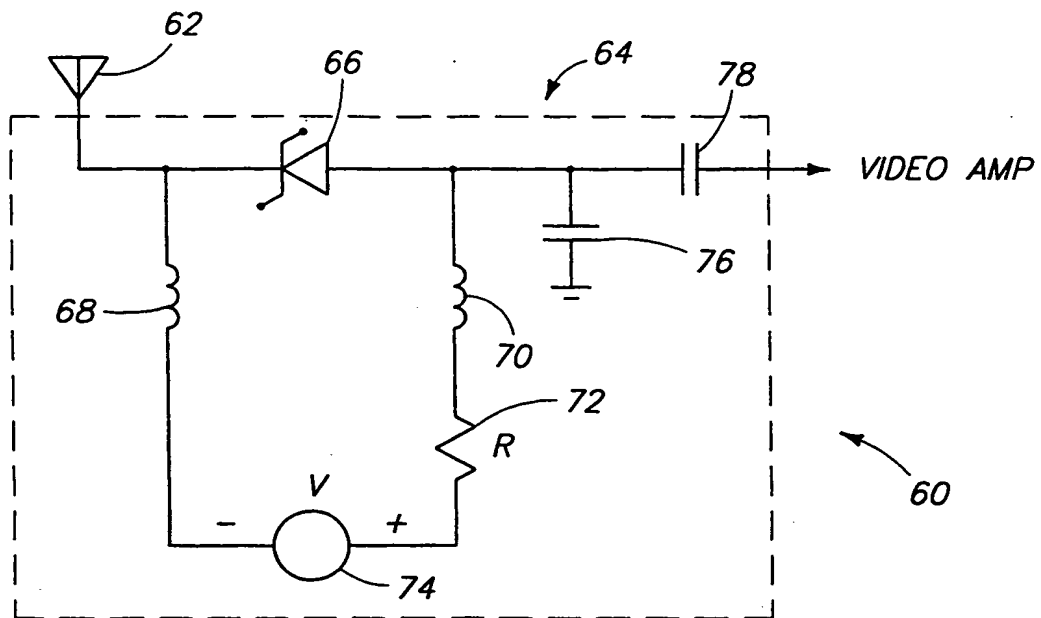


FIG. 28

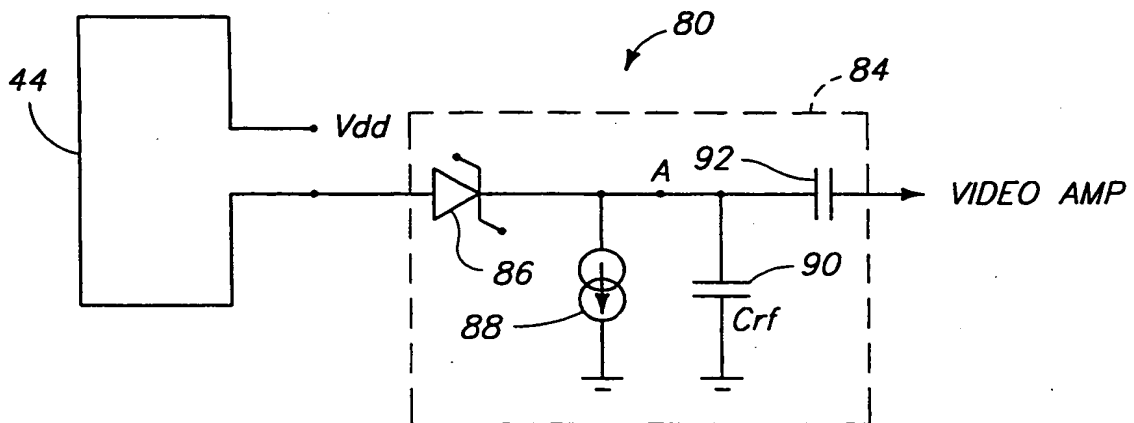
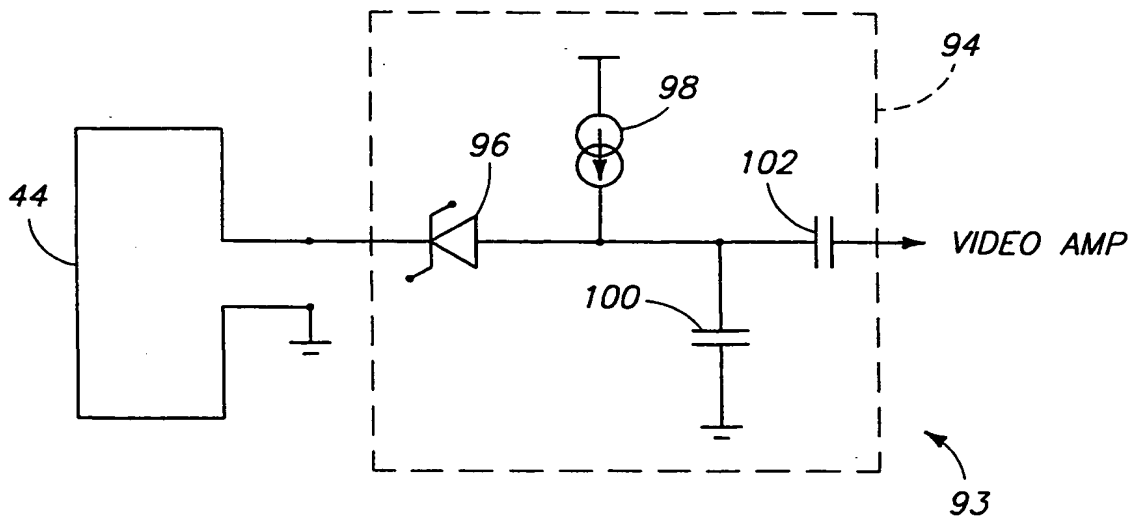
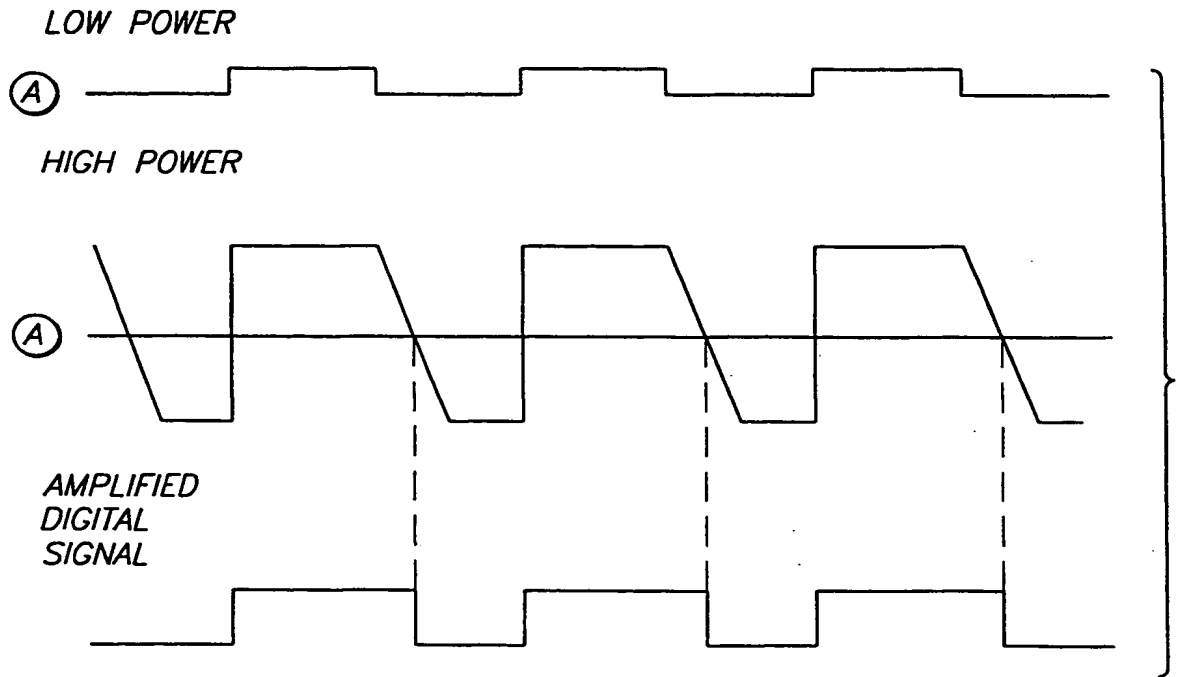


FIG. 29



*II II II II*



*II II II II*

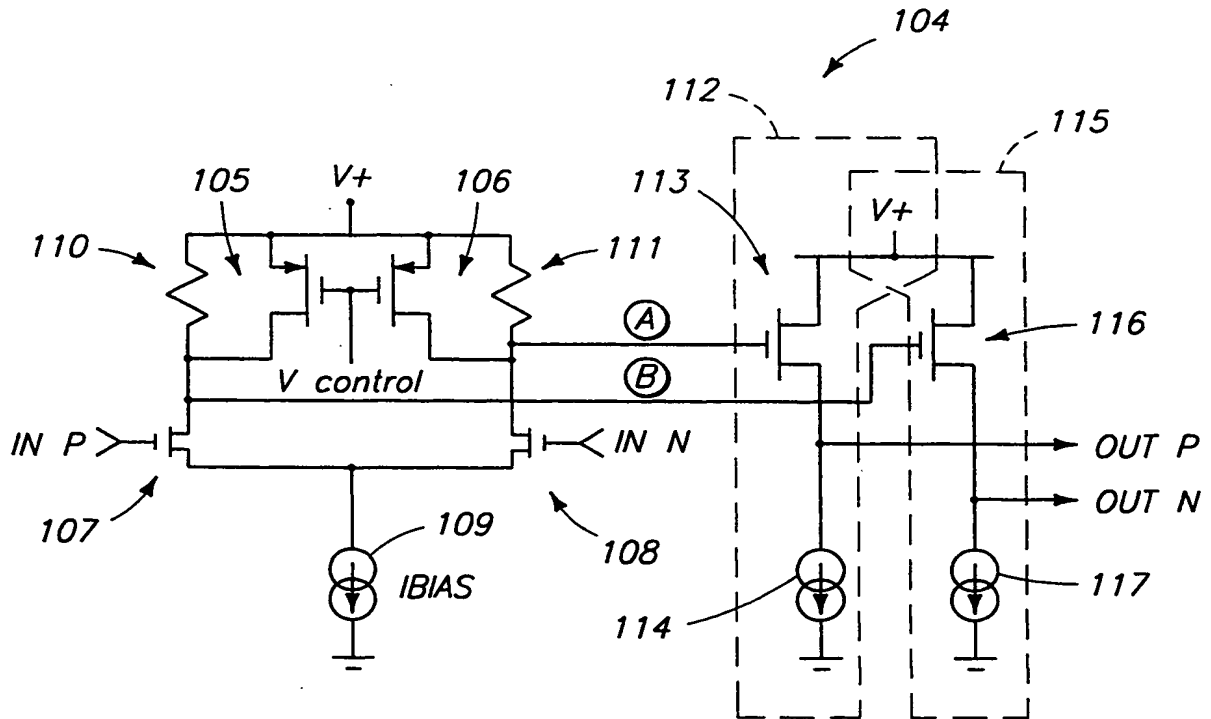


FIG. 32

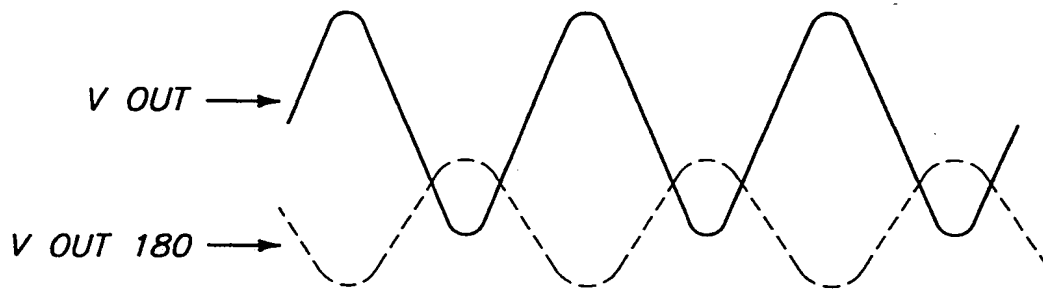
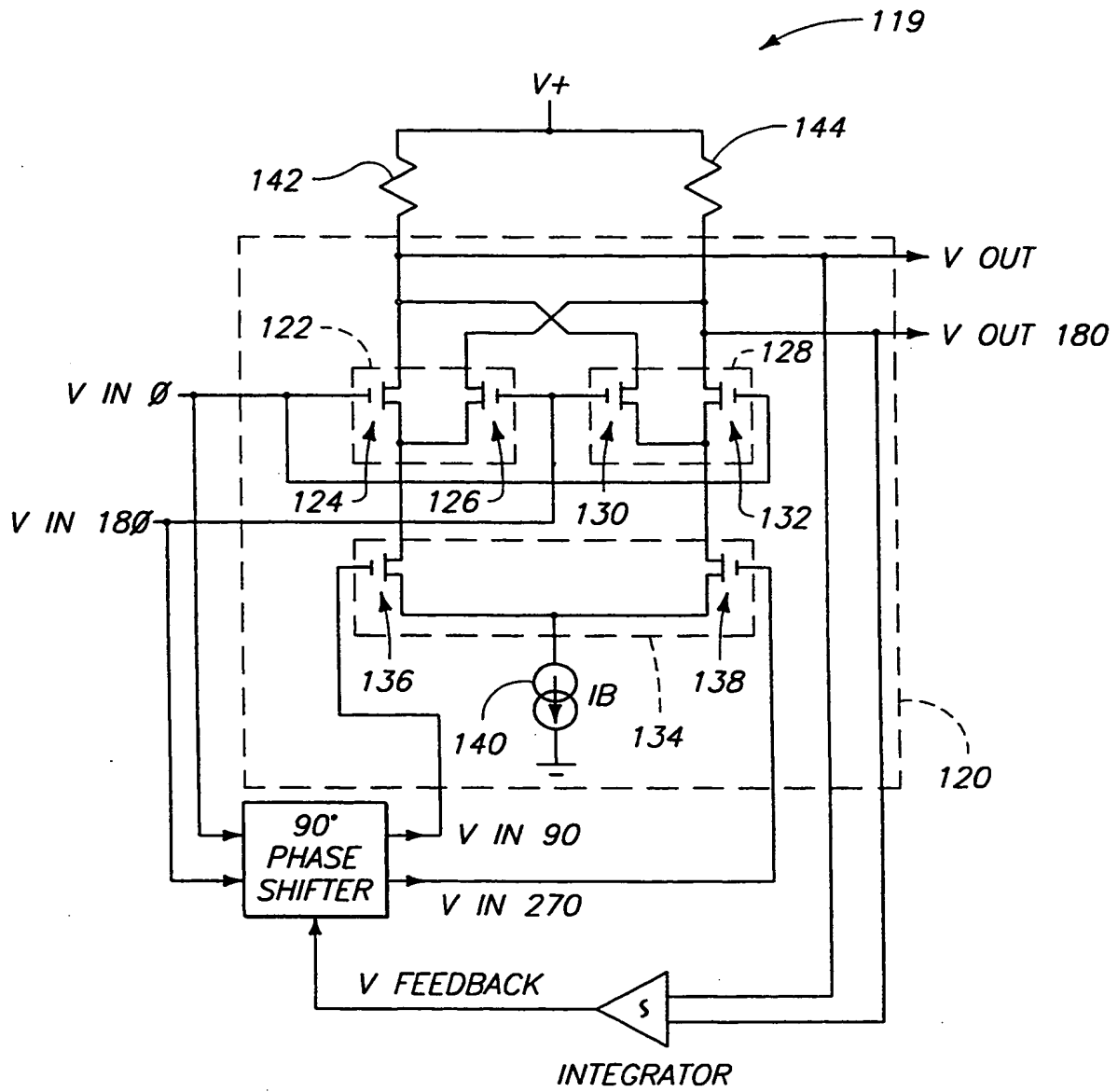
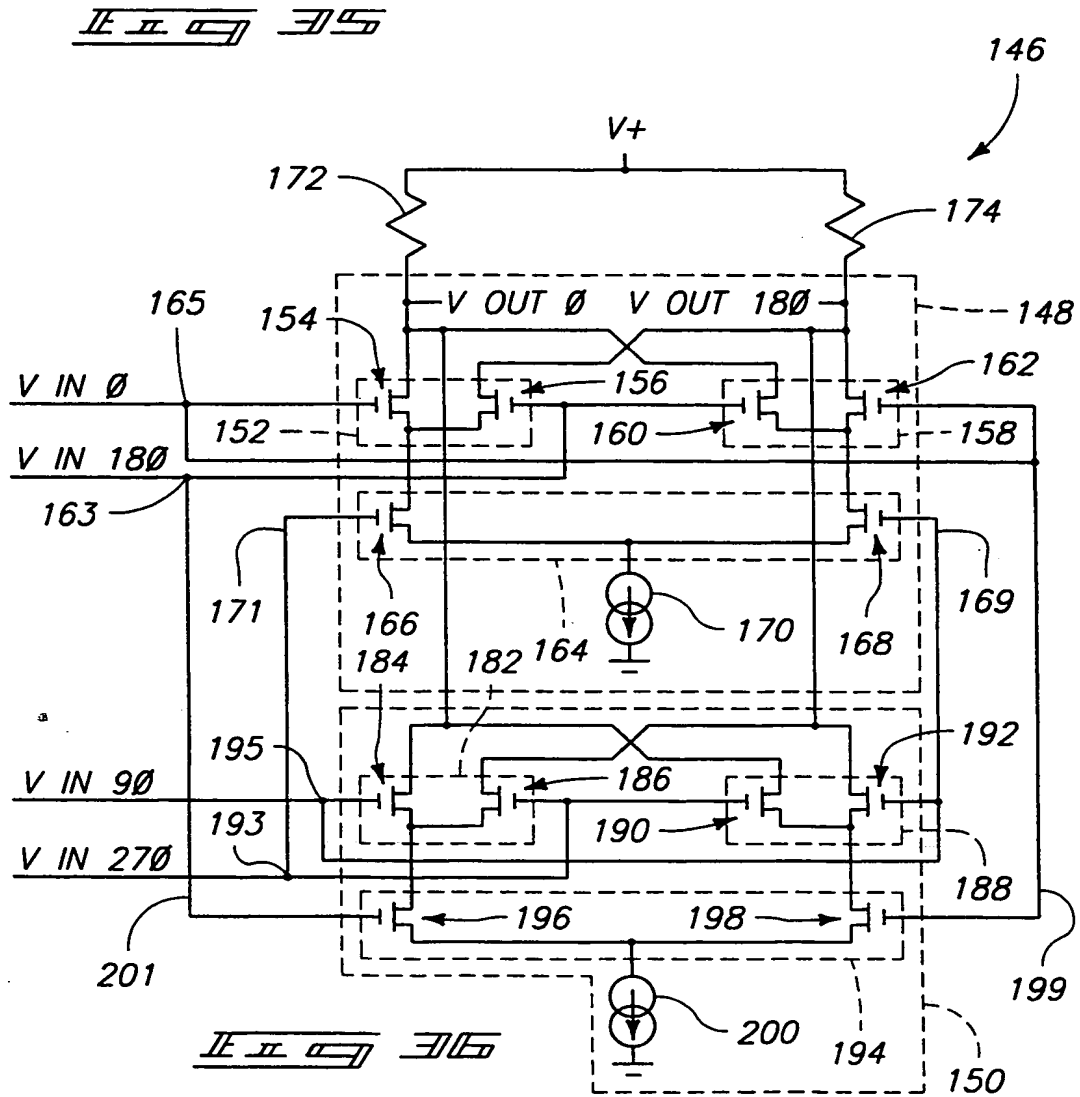
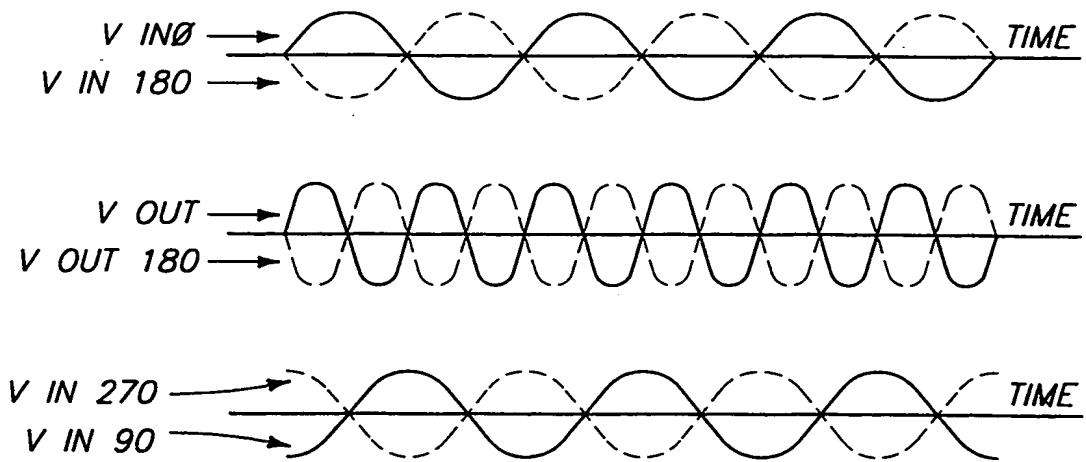


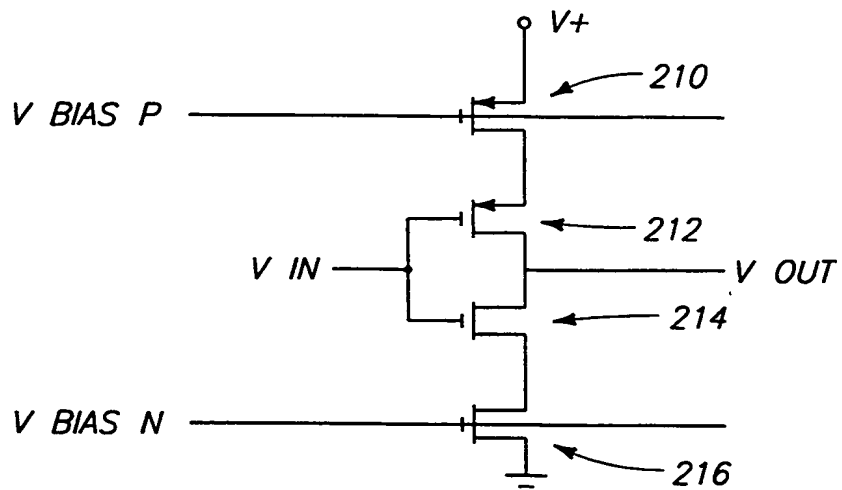
FIG. 33



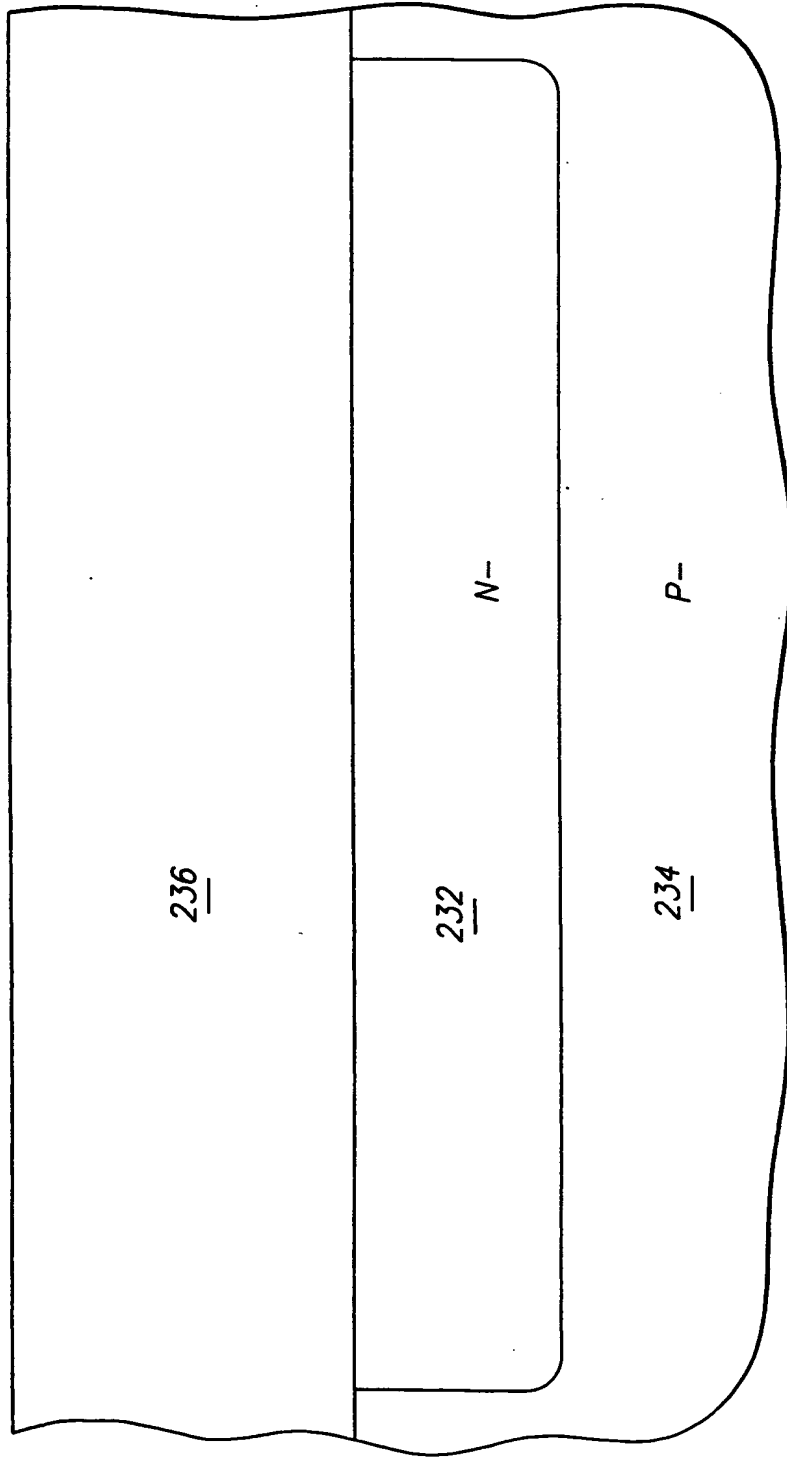
IEEE 304



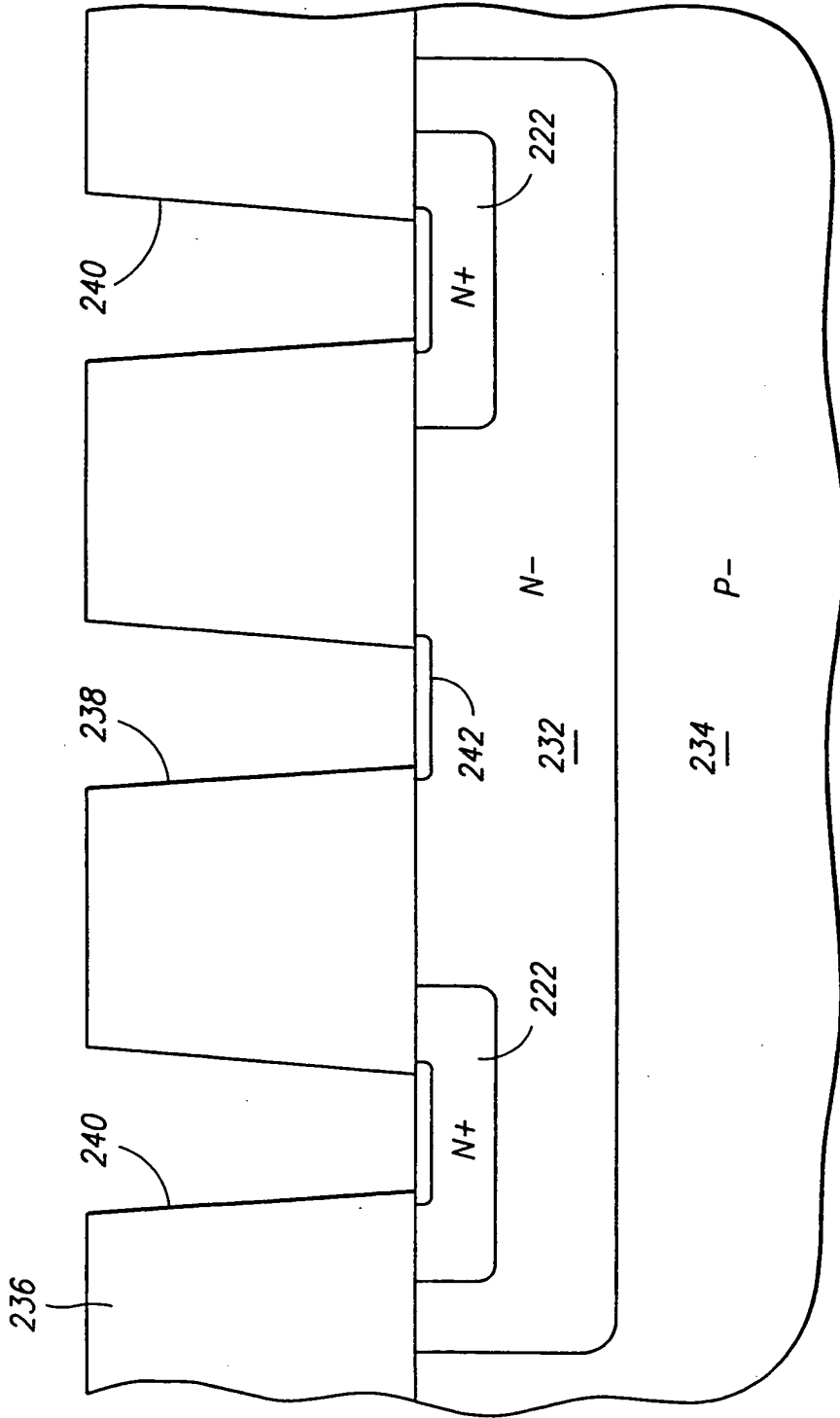




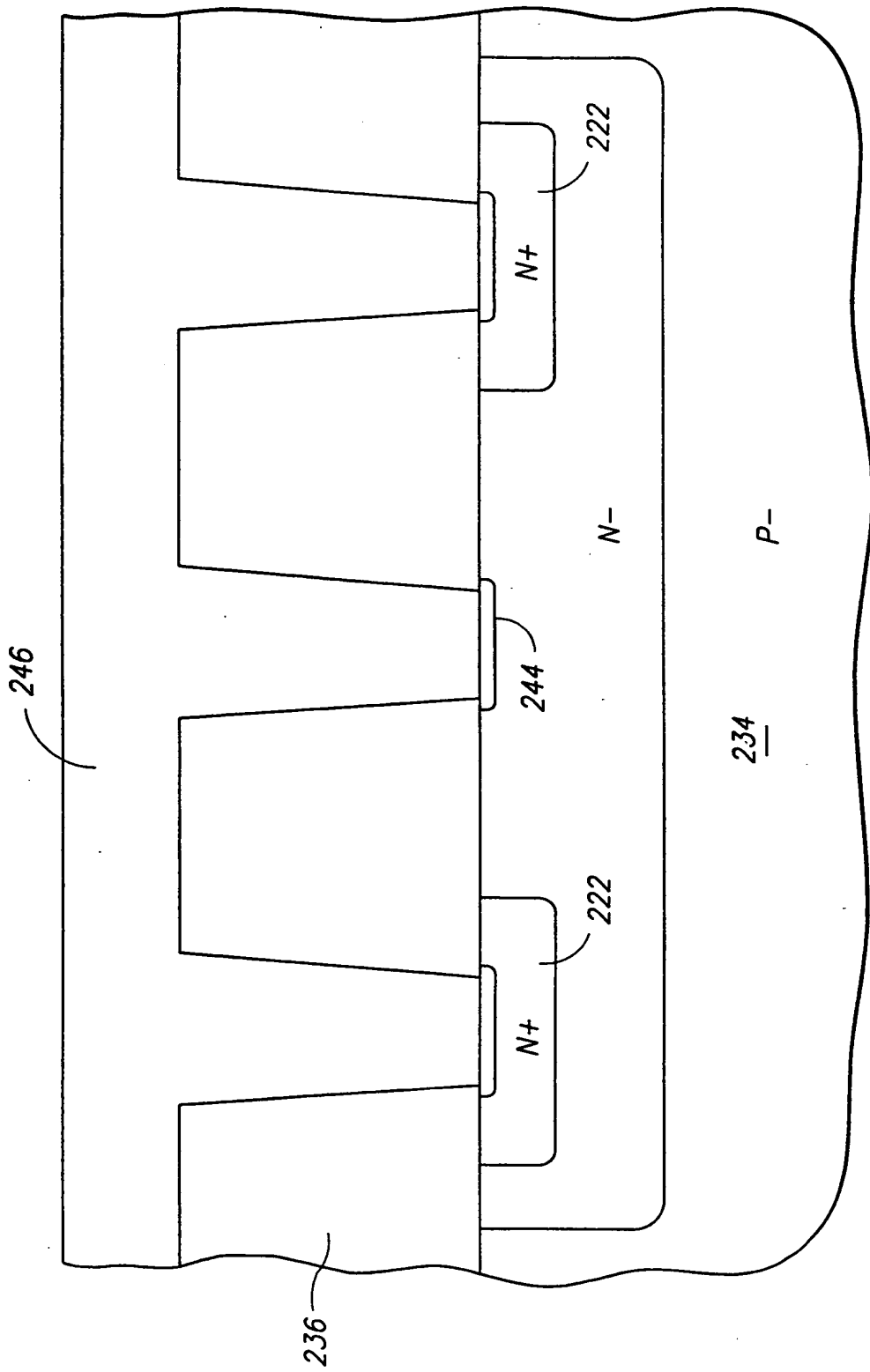
IEEE



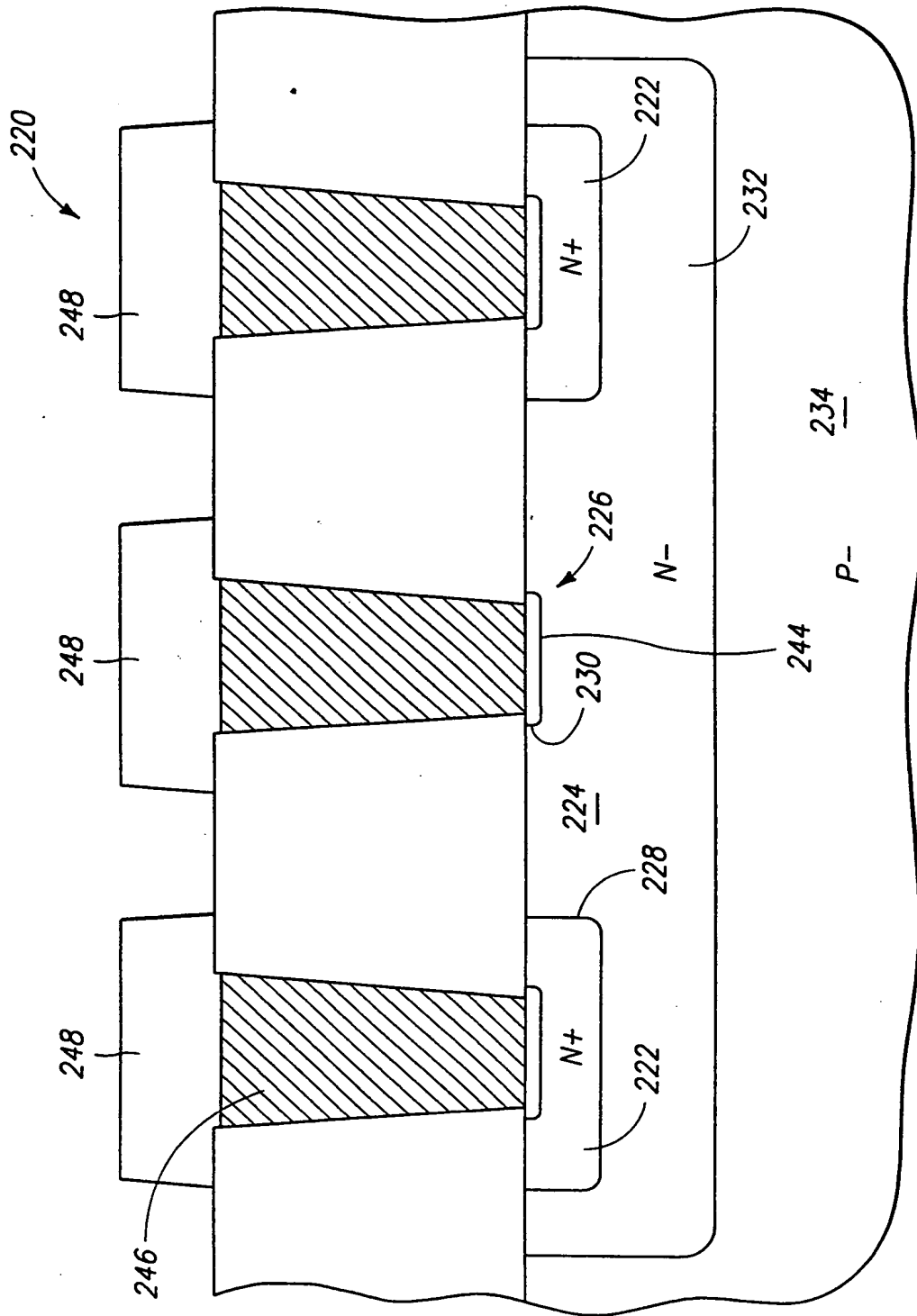
II II II 3188



SEE FIG. 3



MI 40-030



MI 40-030

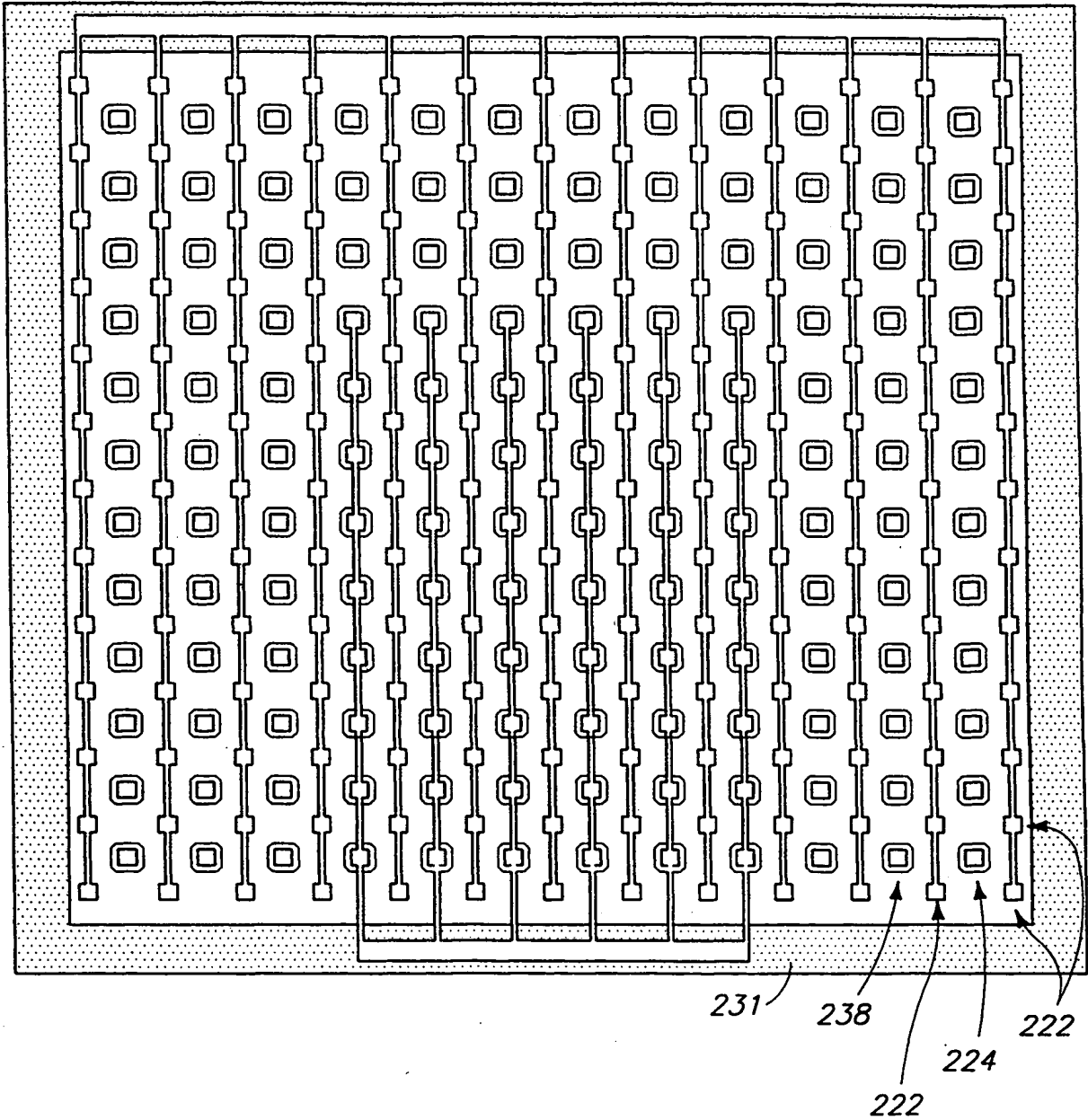
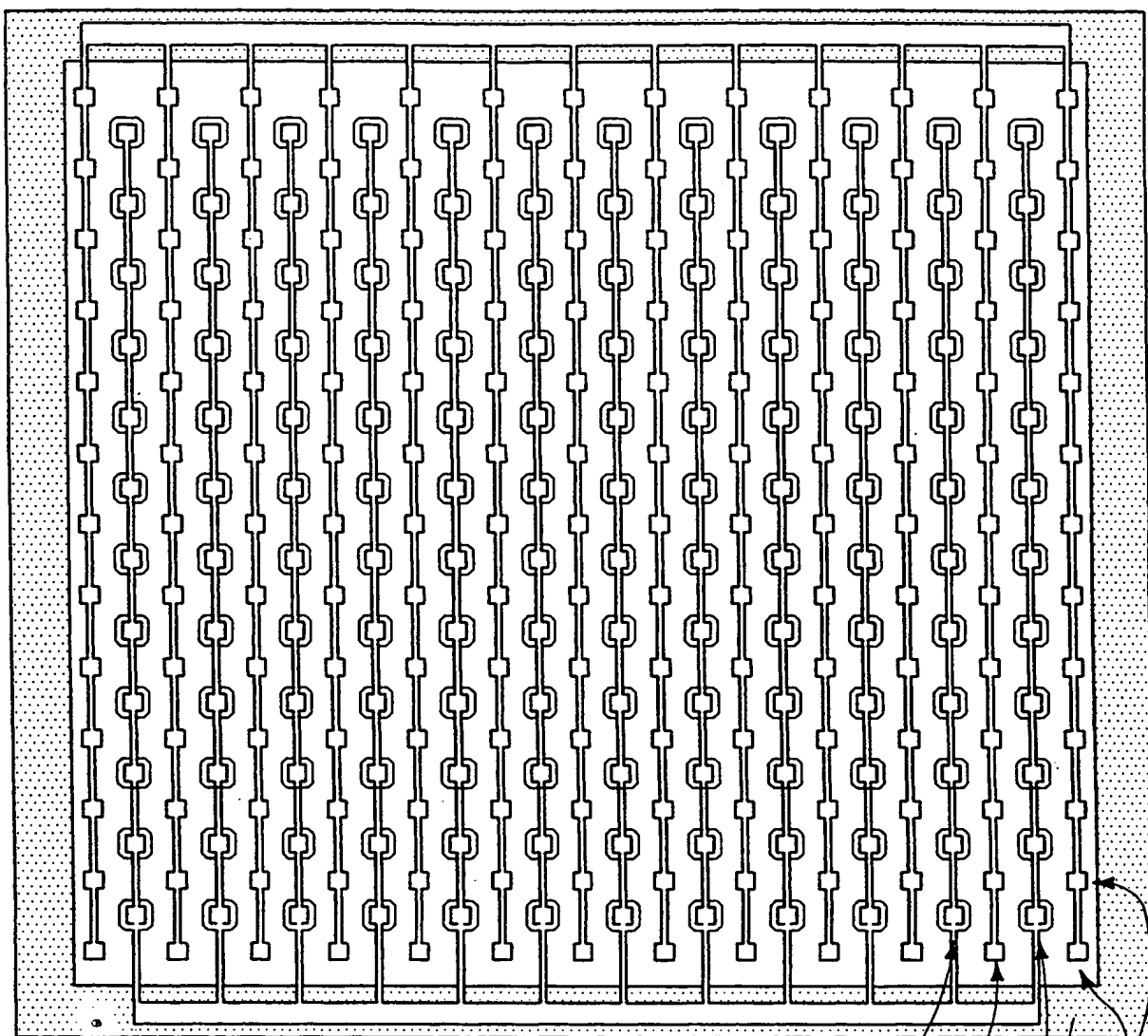


FIG. 4



238  
224  
222  
231  
222

FIG. 4



260

258

P-

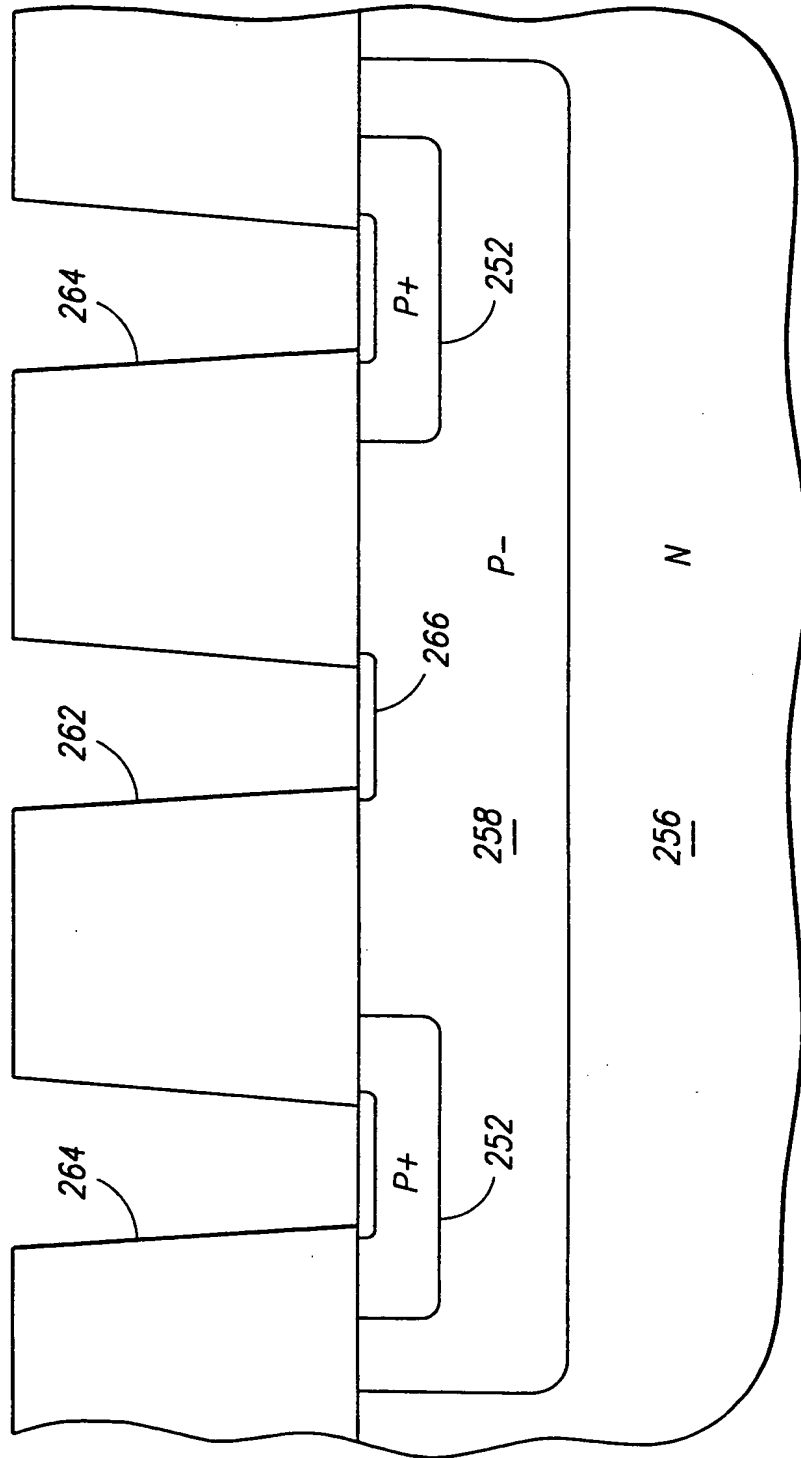
256

N

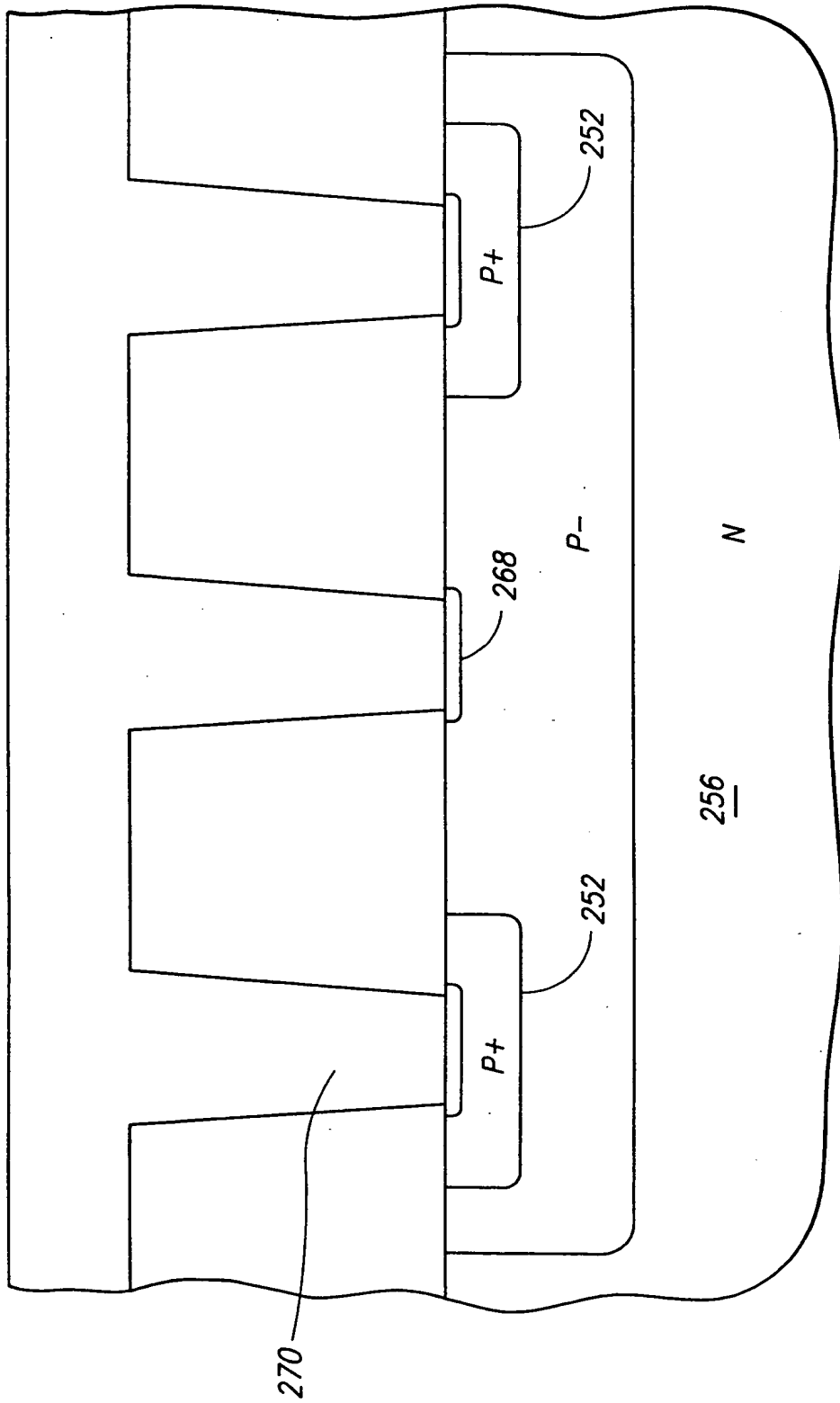
P.

$$\geq$$

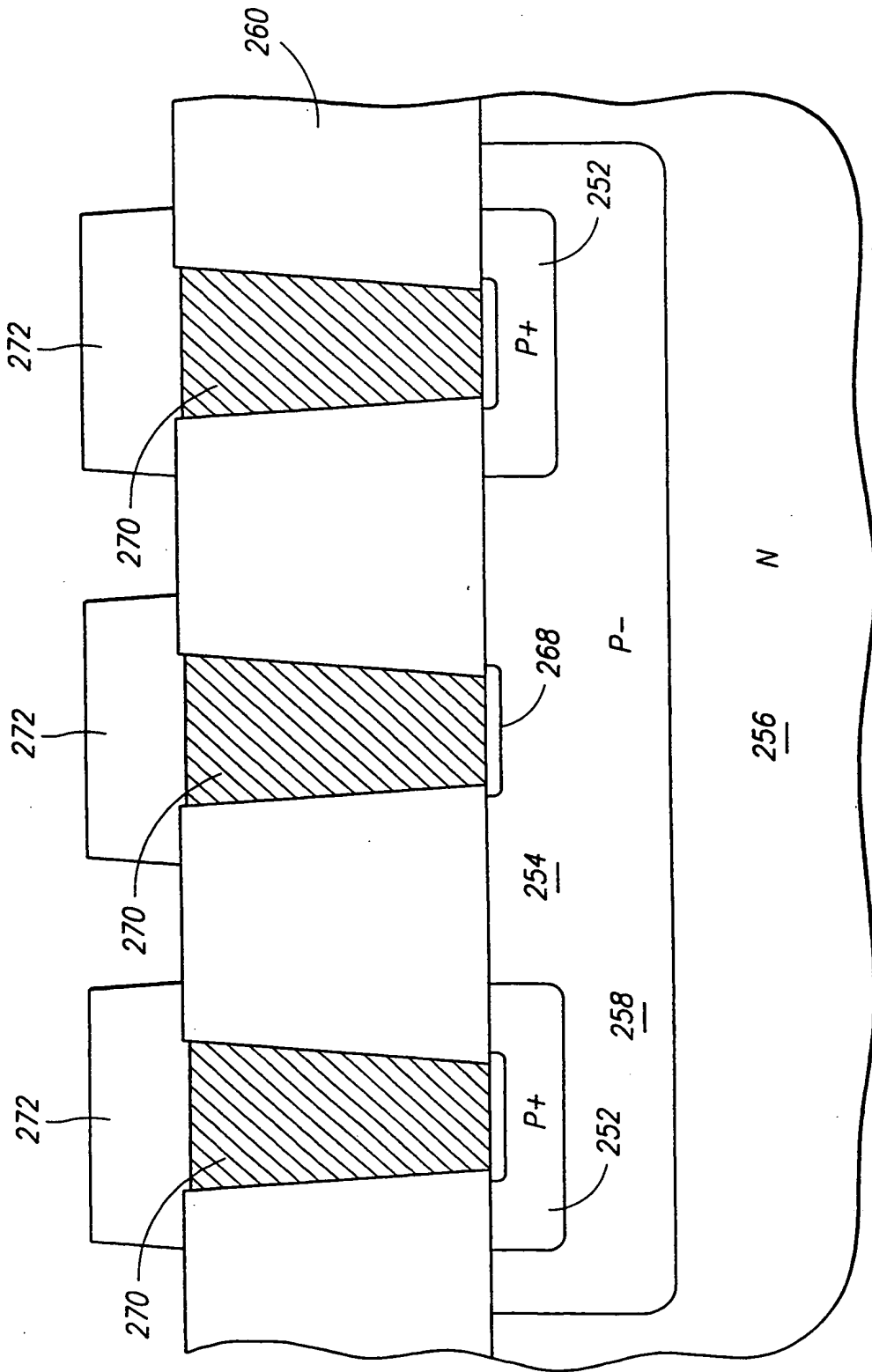
# Борис



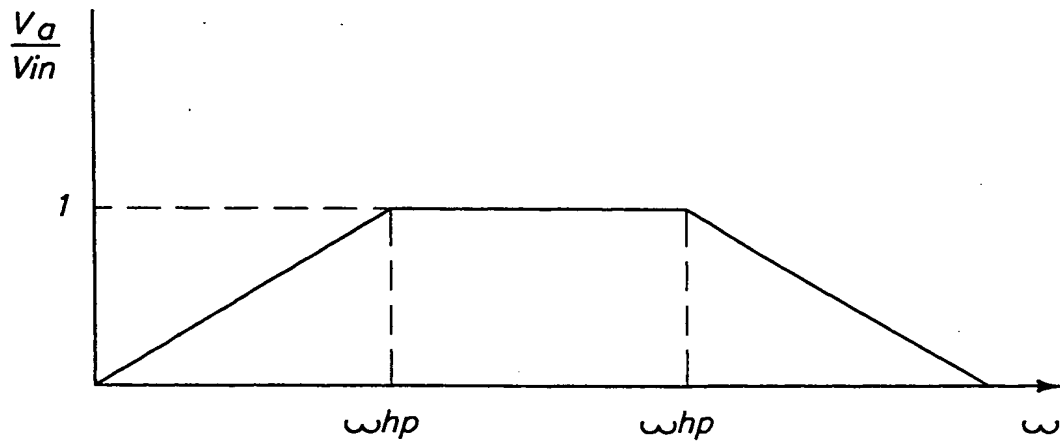
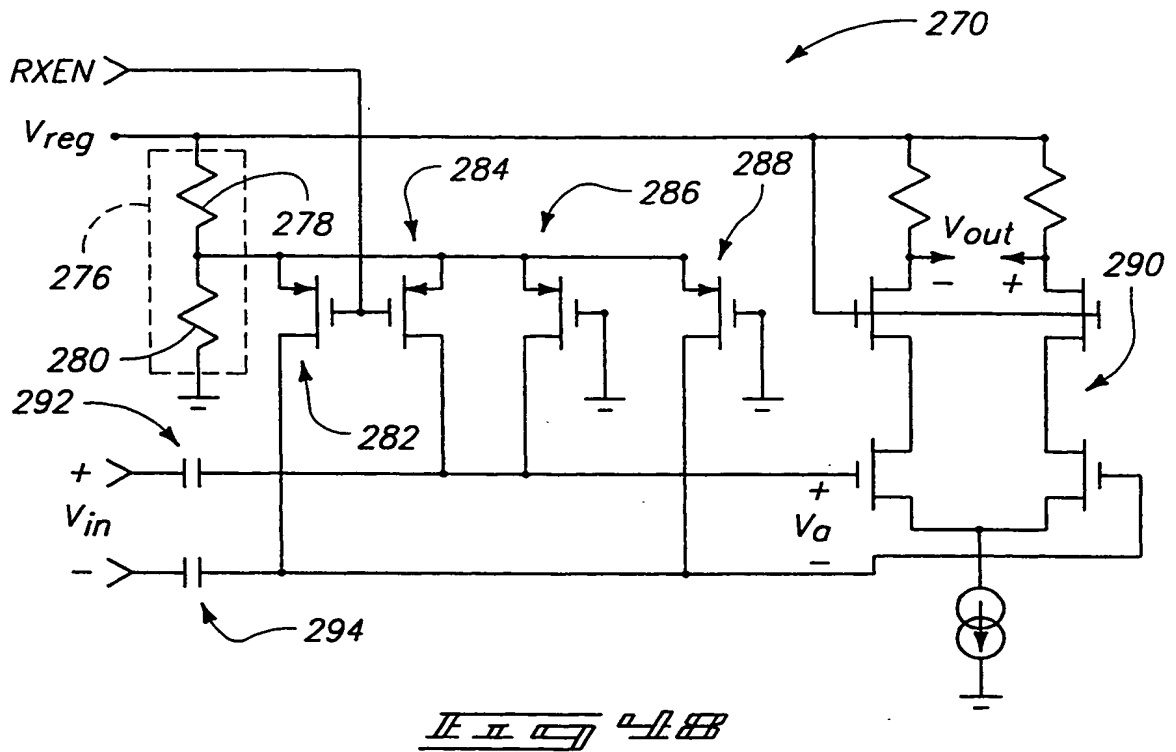
MI40-030



MI 40



MI 40-030



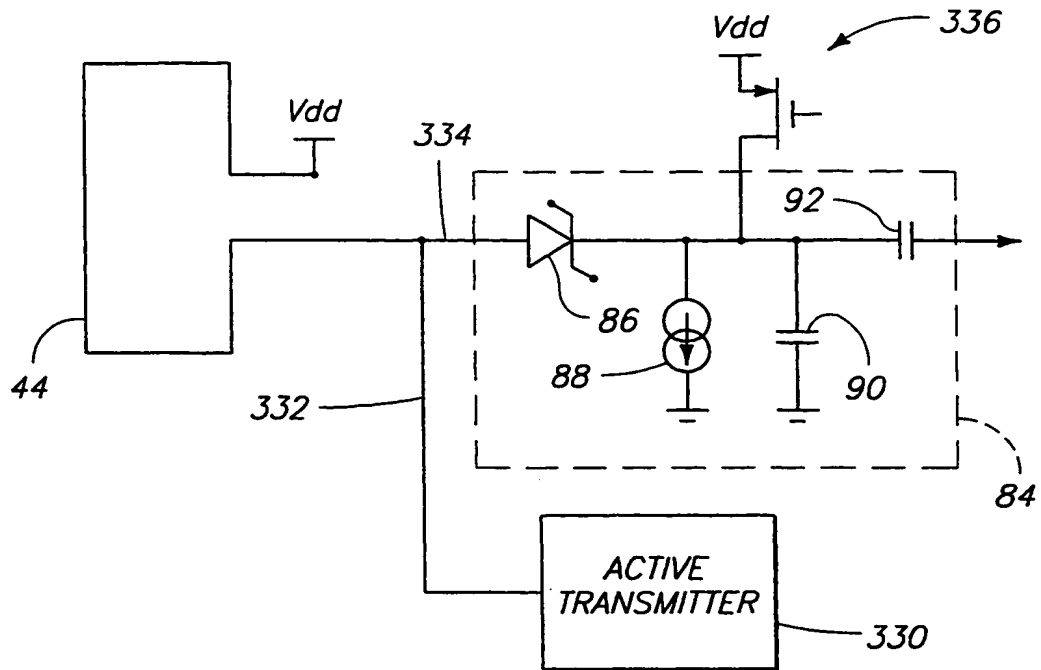


FIG 50

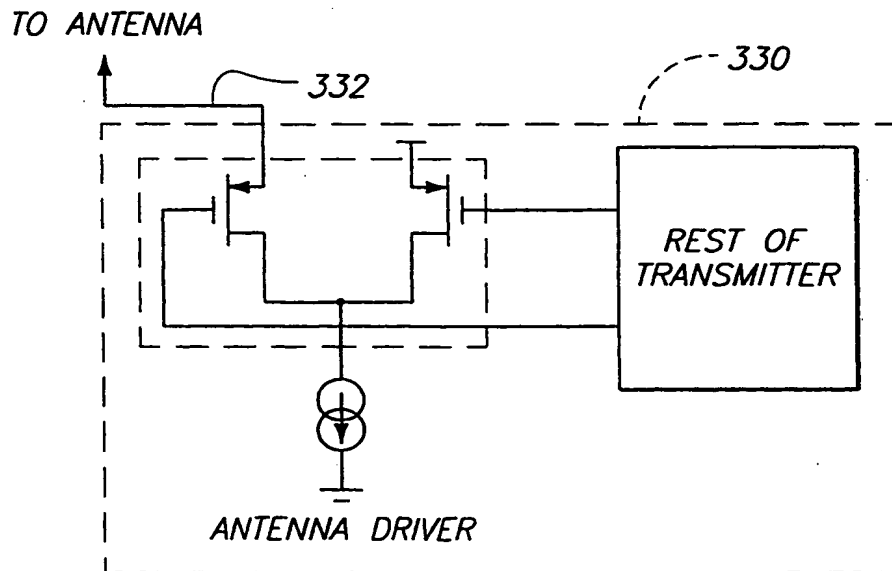


FIG 51

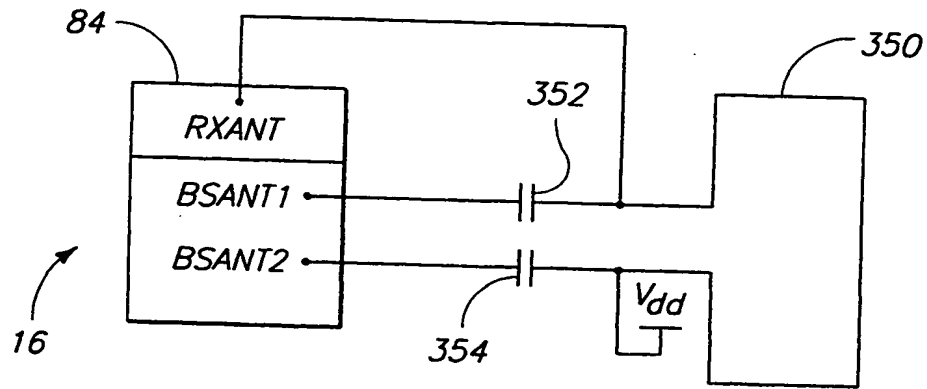


FIG. 52

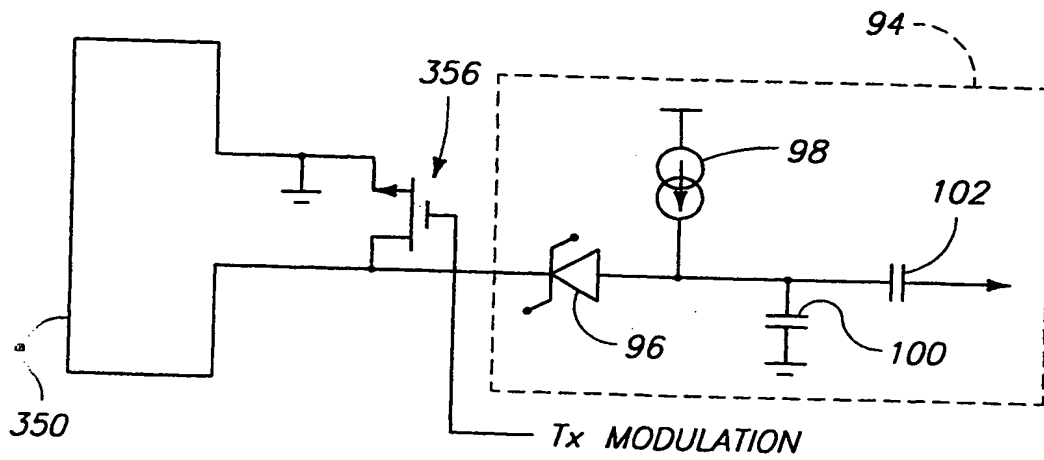
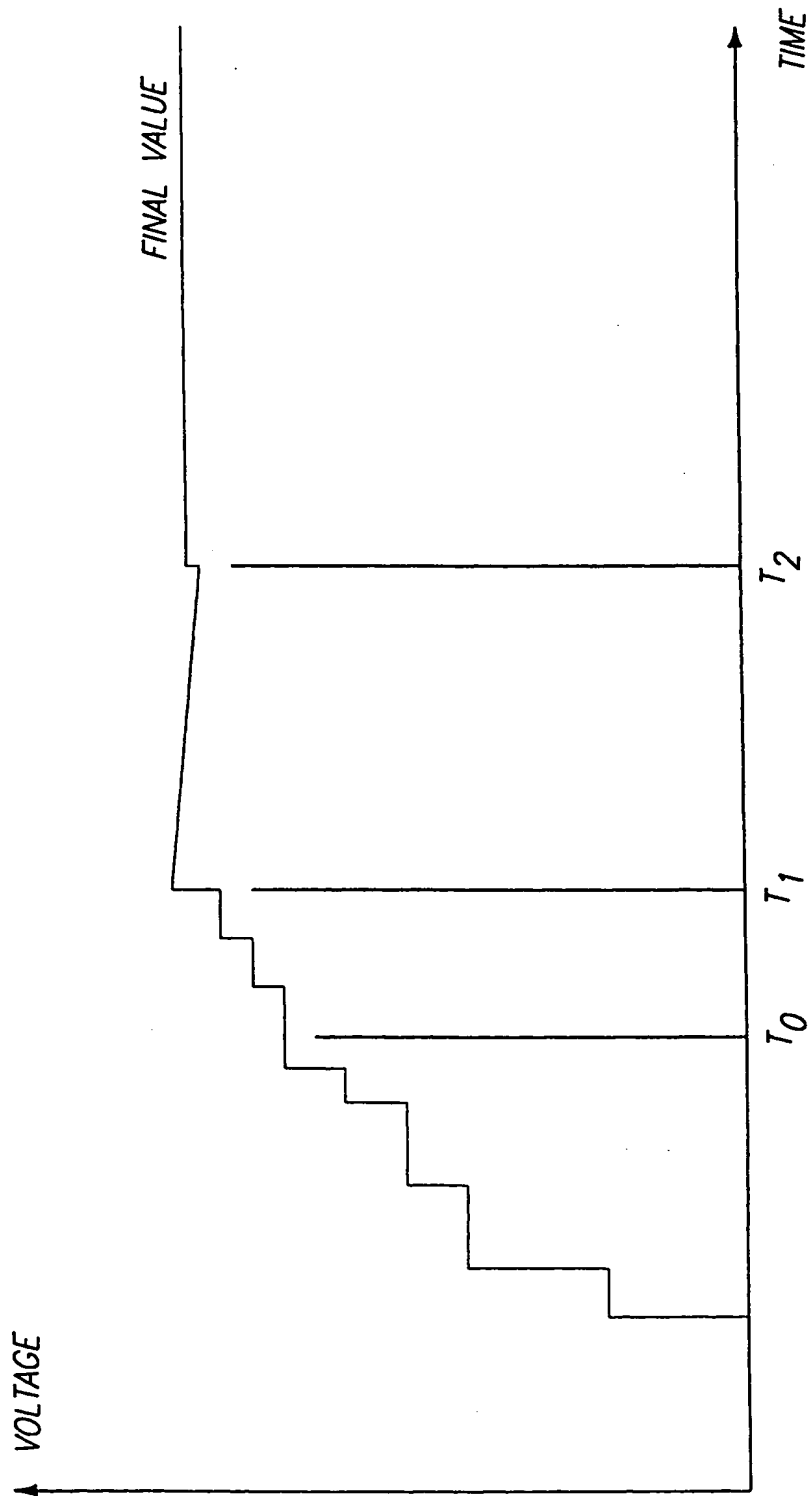
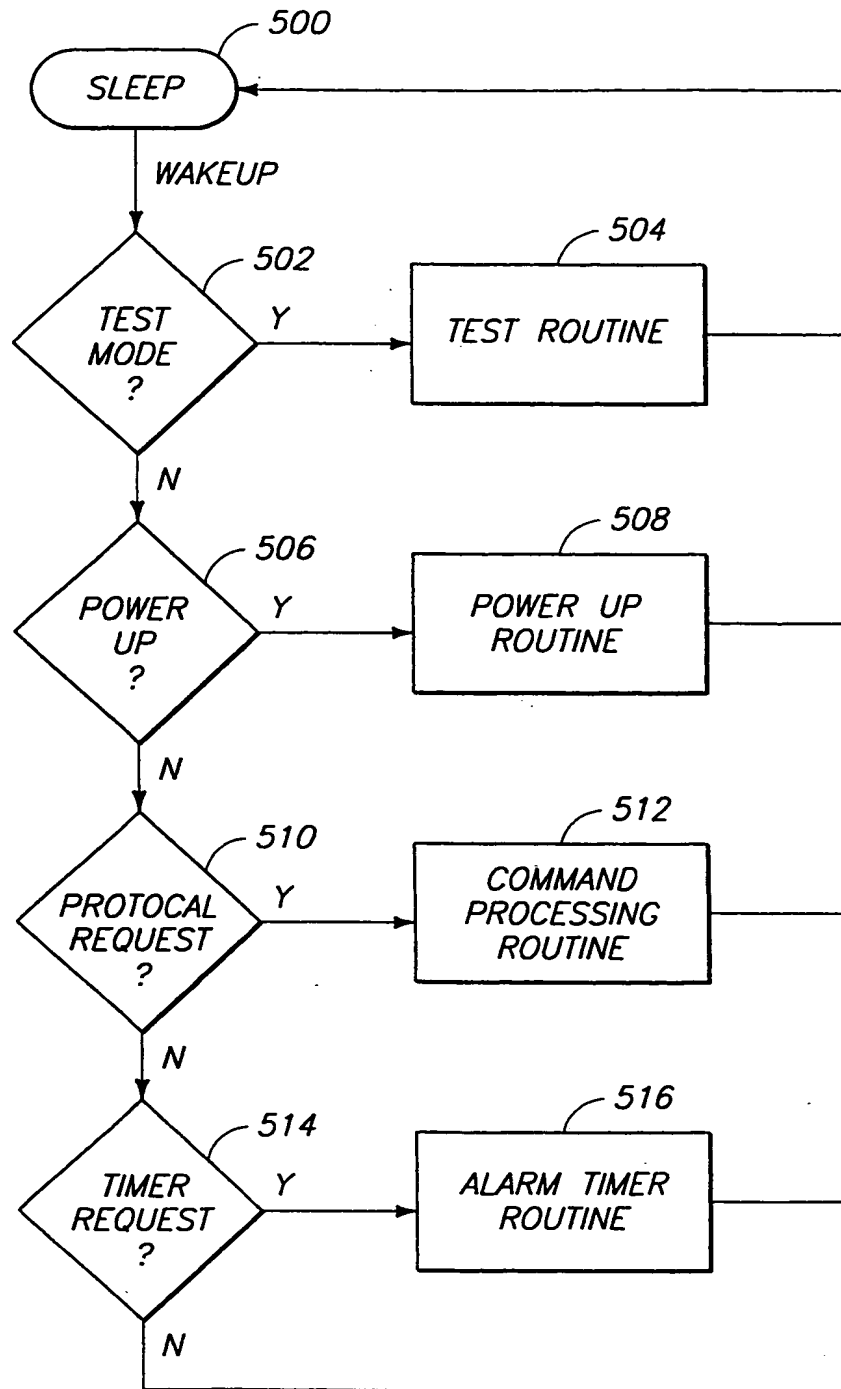


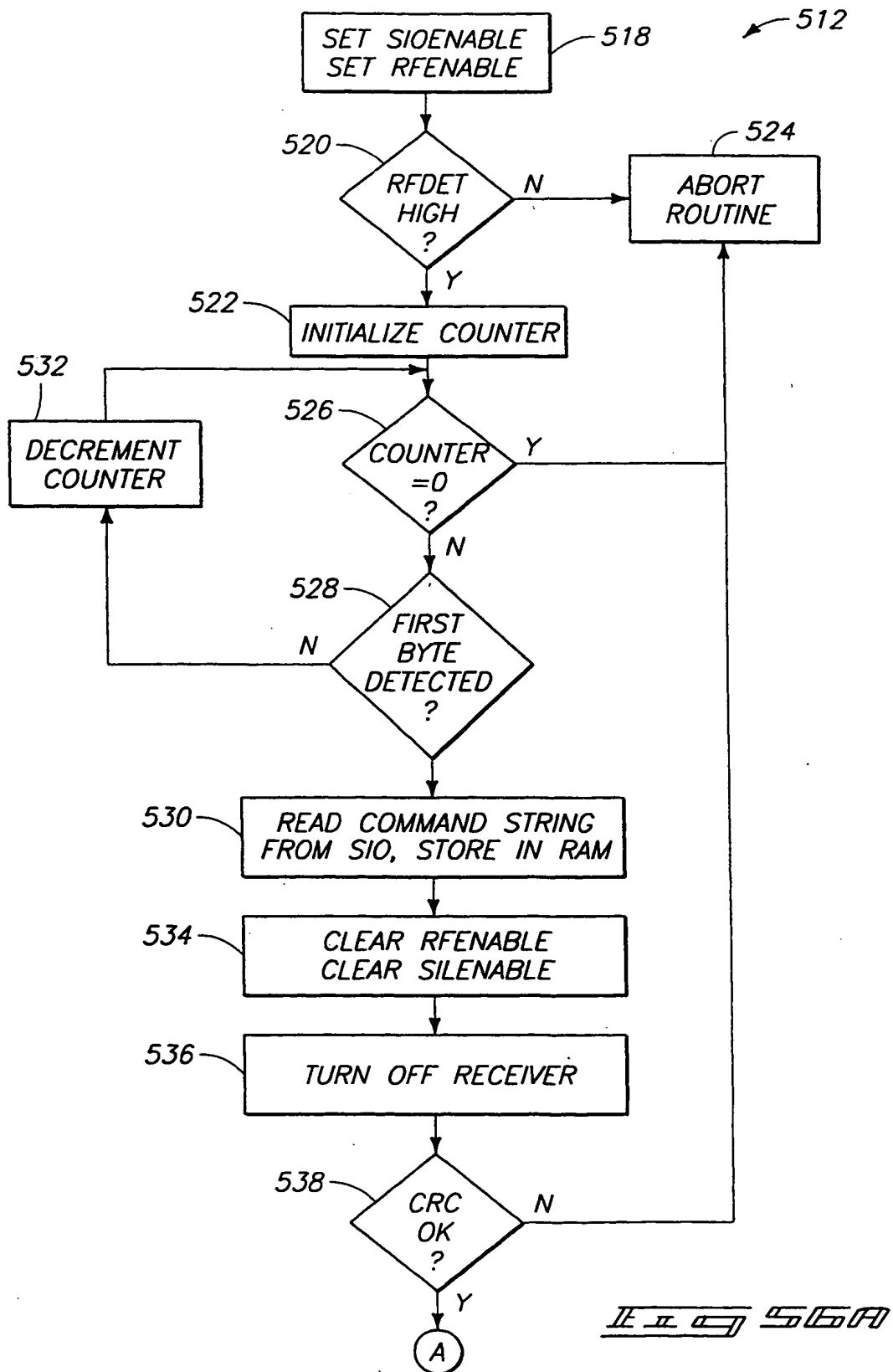
FIG. 53

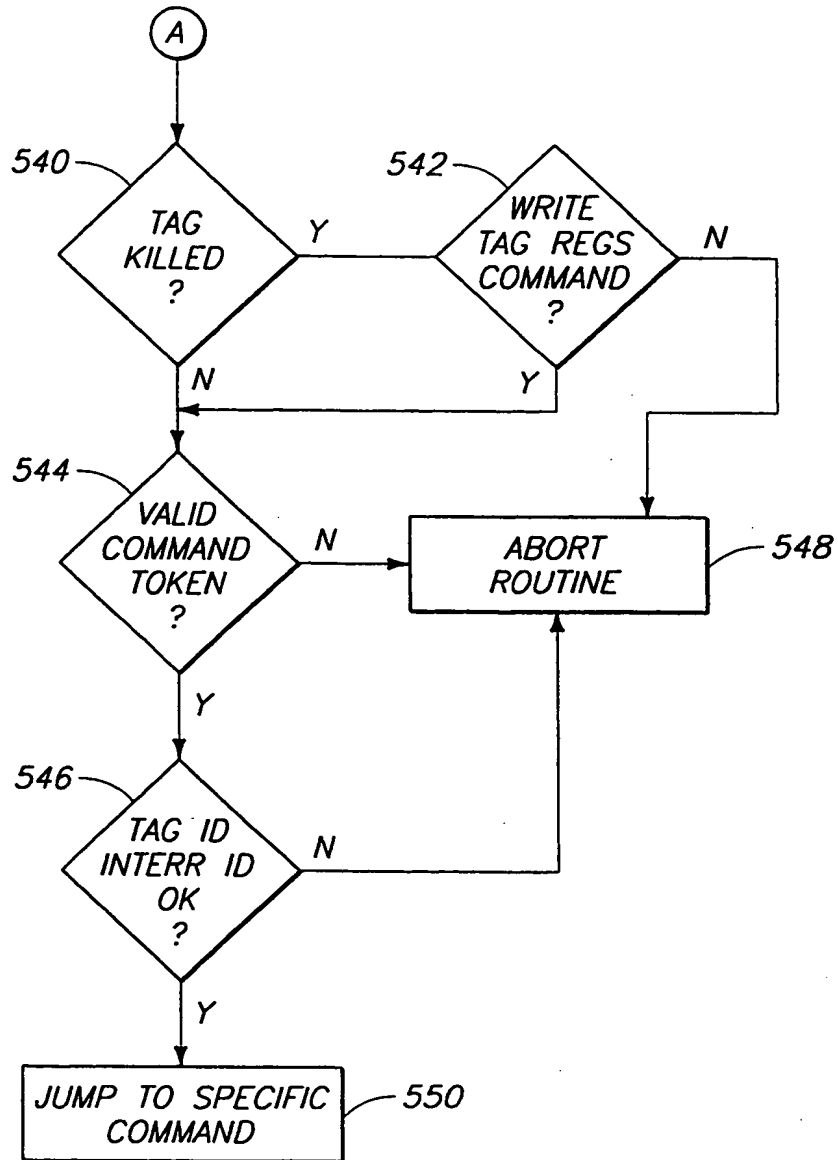


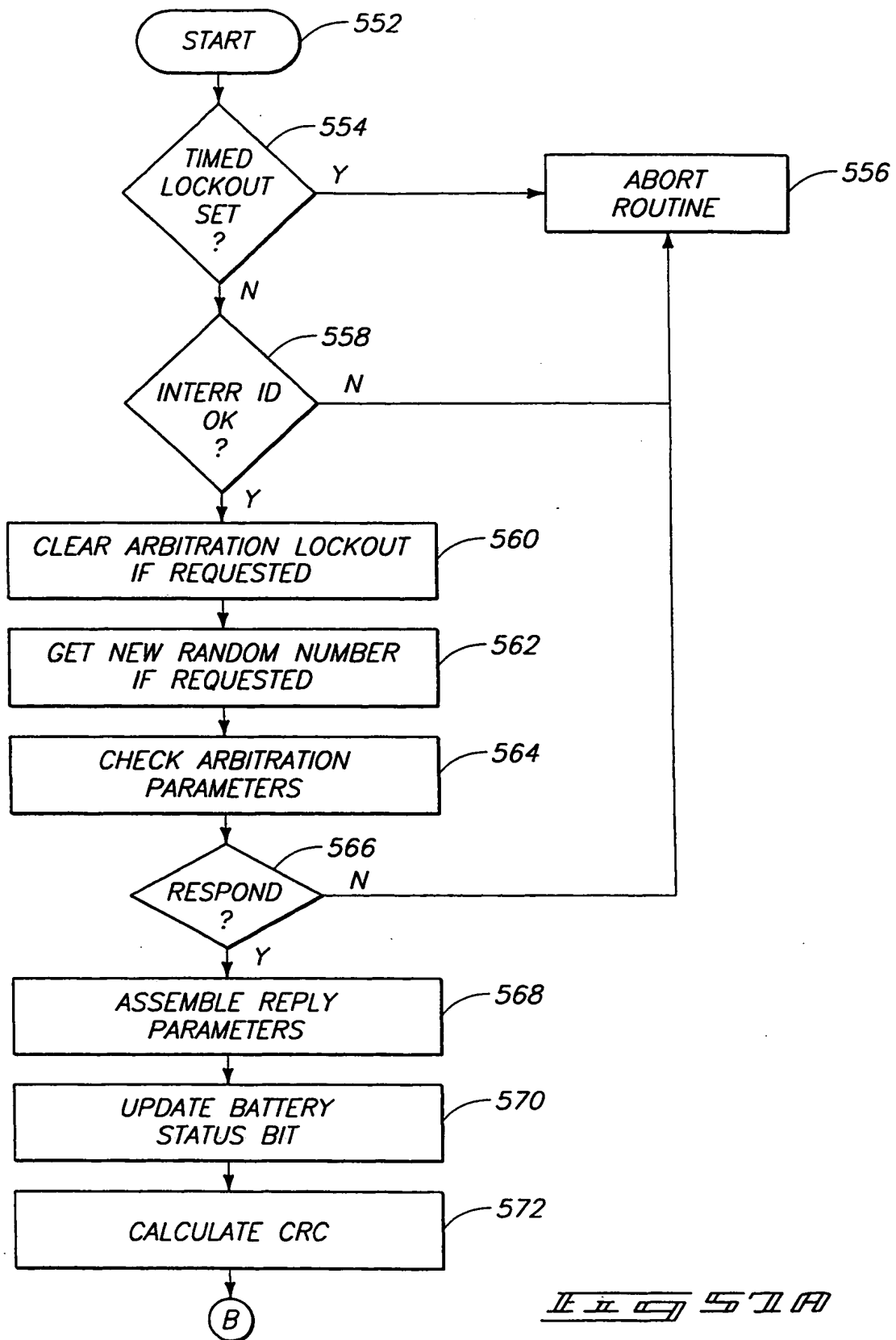
TEST DATA

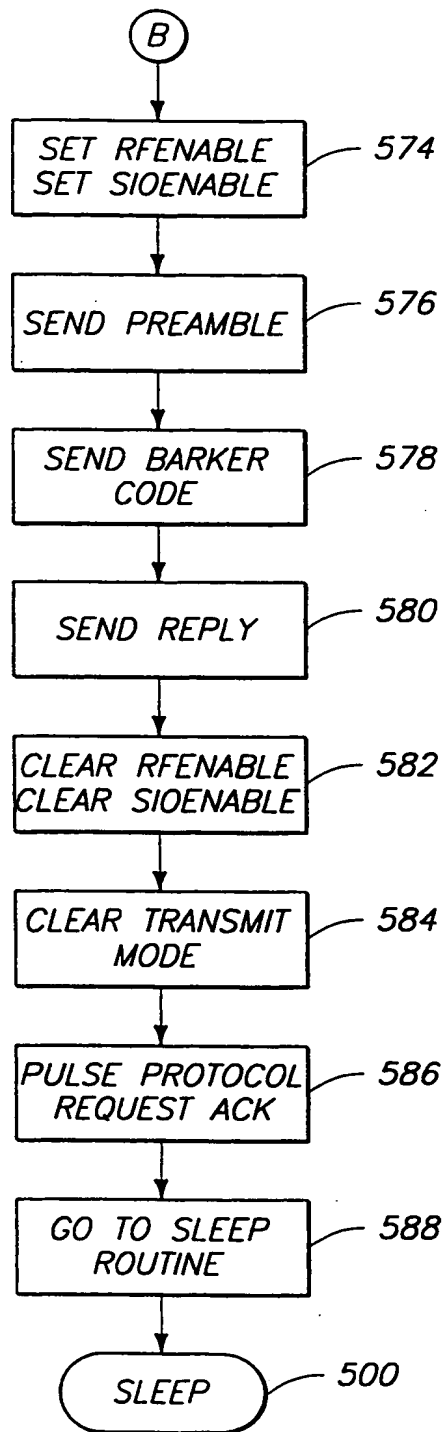


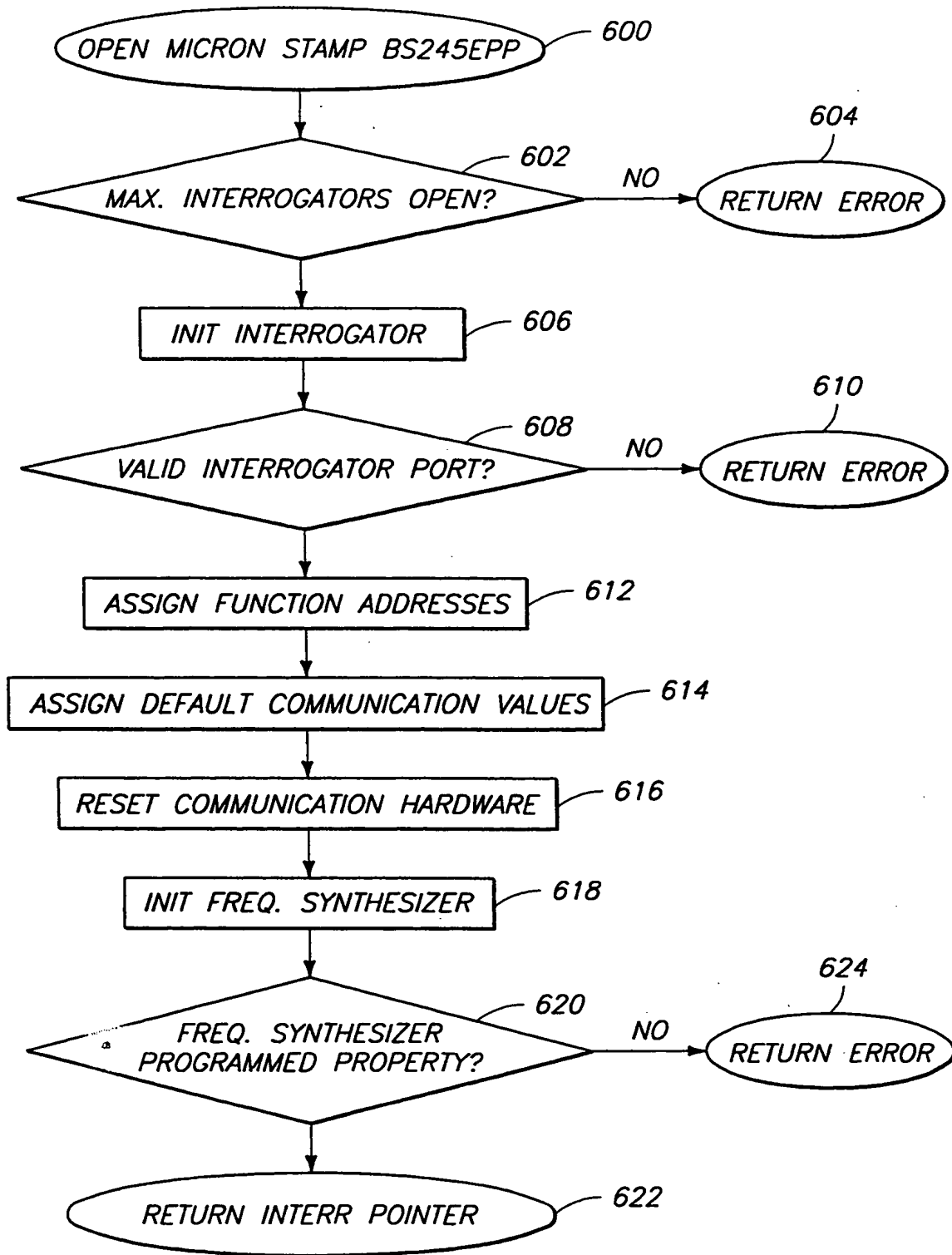


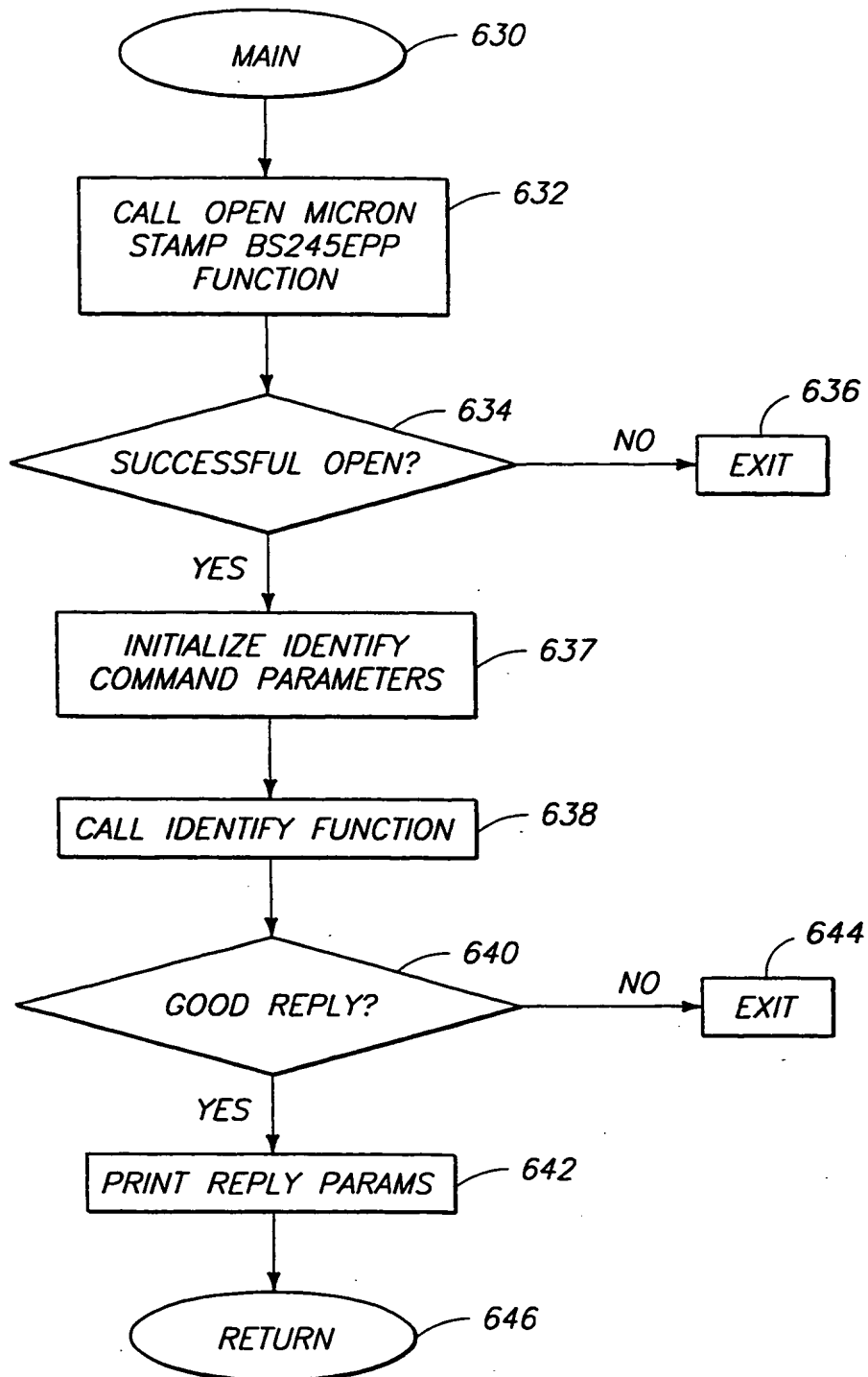


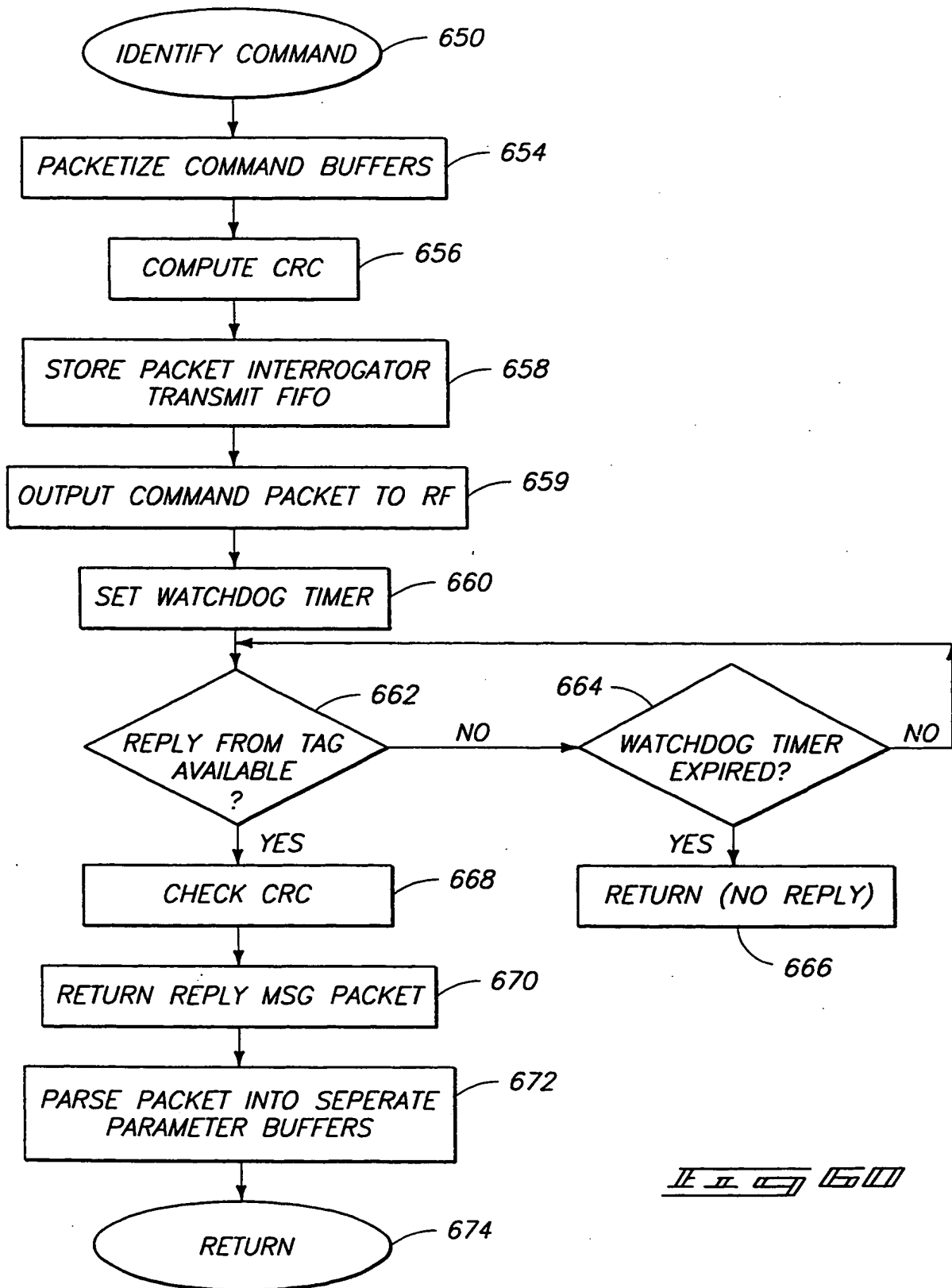
IEEE 56B





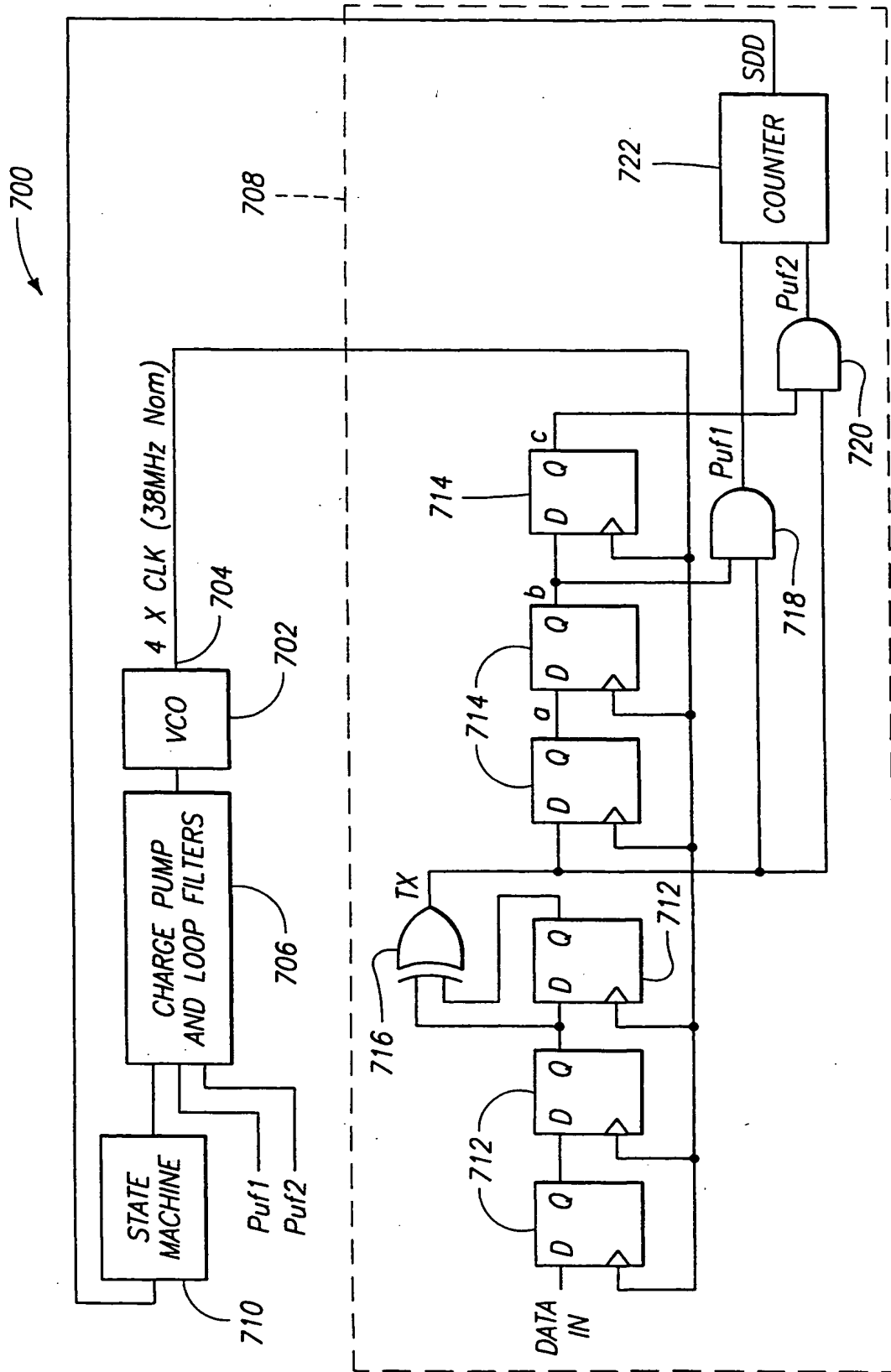






II 5 60





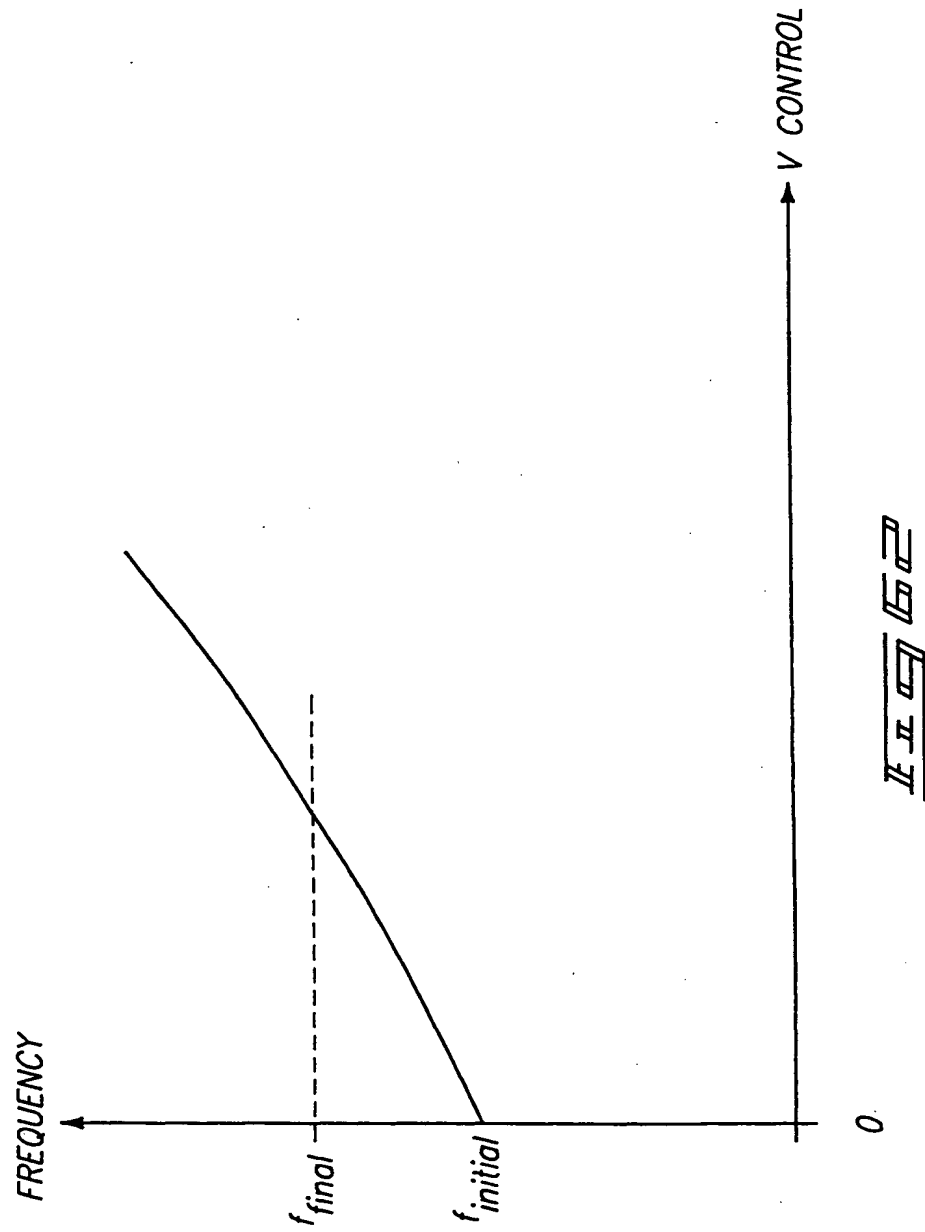


Fig 62

1 1 0 0 1 0 1 1 0 1 1 1 0 1 0 1 0 1 0 0 0 1 0 0 0 1 1 1 0 0 0 0

CHIP SEQUENCE  
FOR "0" BIT

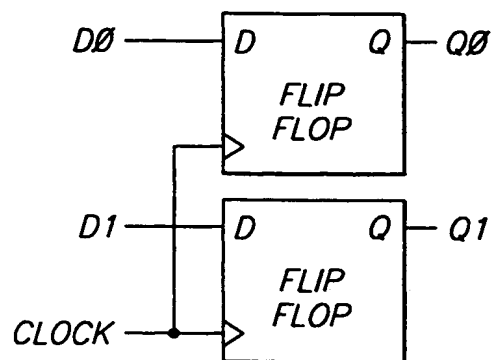
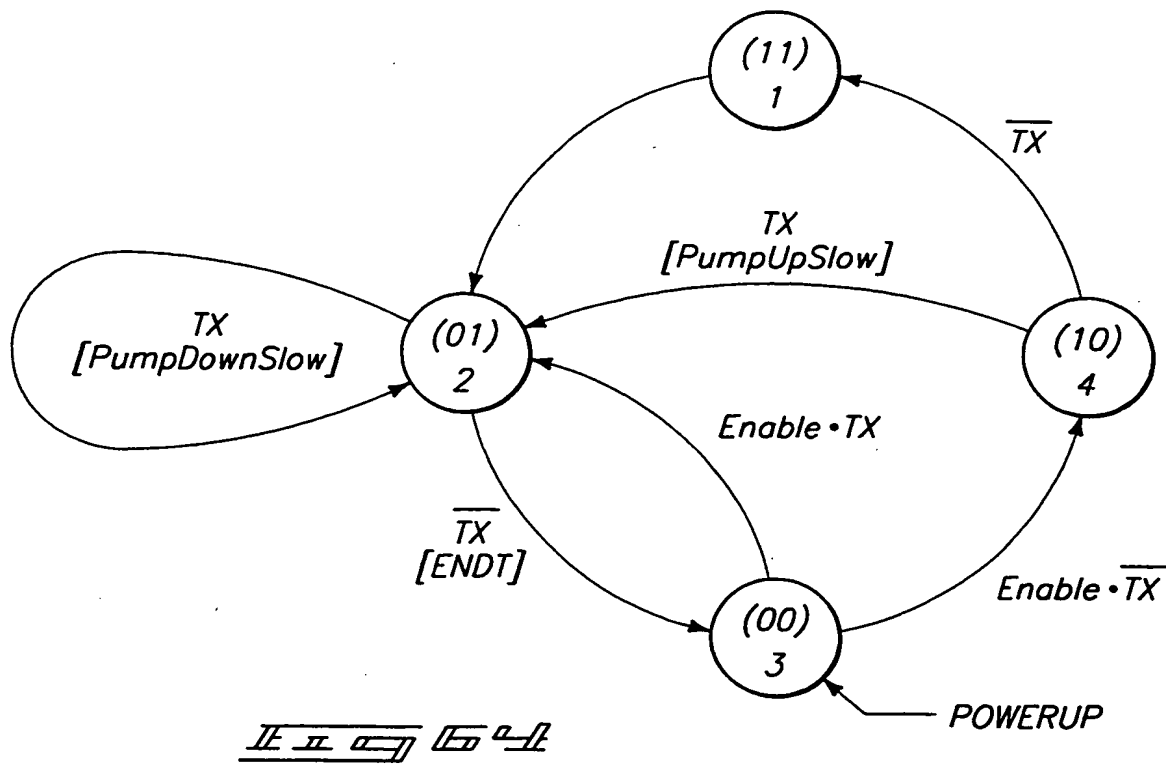
VCO OUT (50%)

TX

TX DELAYED  
2 CYCLES

Puf1

Figure 1



IEEE Std 635

	PRESENT STATE				NEXT STATE	
	ENABLE	TX	Q1	Q0	D1	D0
0	0	0	0	0	0	0
0	0	1	0	0	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
X	X	0	0	1	0	0
X	X	1	0	1	0	1
X	X	X	1	1	0	1
X	X	0	1	0	1	1
X	X	1	1	0	0	1

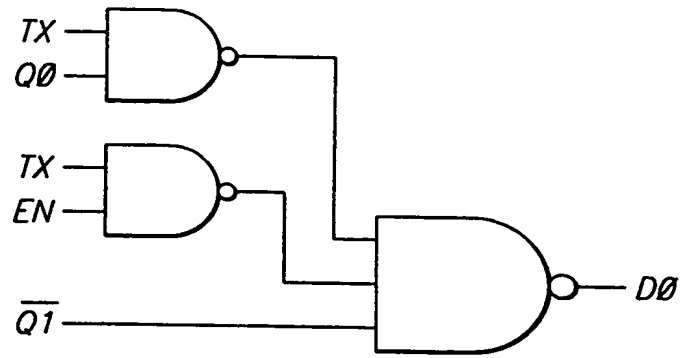
EX 66

En TX		Q1 Q0			
		00	01	11	10
D0:	00	0	0	1	1
	01	0	1	1	1
	11	1	1	1	1
	10	0	0	1	1

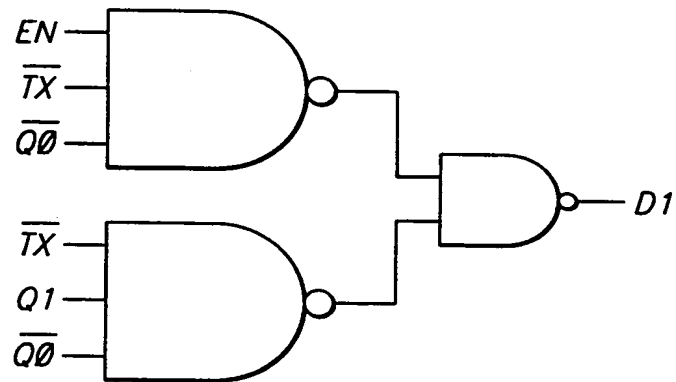
IEEE 67

En TX		Q1 Q0			
		00	01	11	10
D1:	00	0	0	0	1
	01	0	0	0	0
	11	0	0	0	0
	10	1	0	0	1

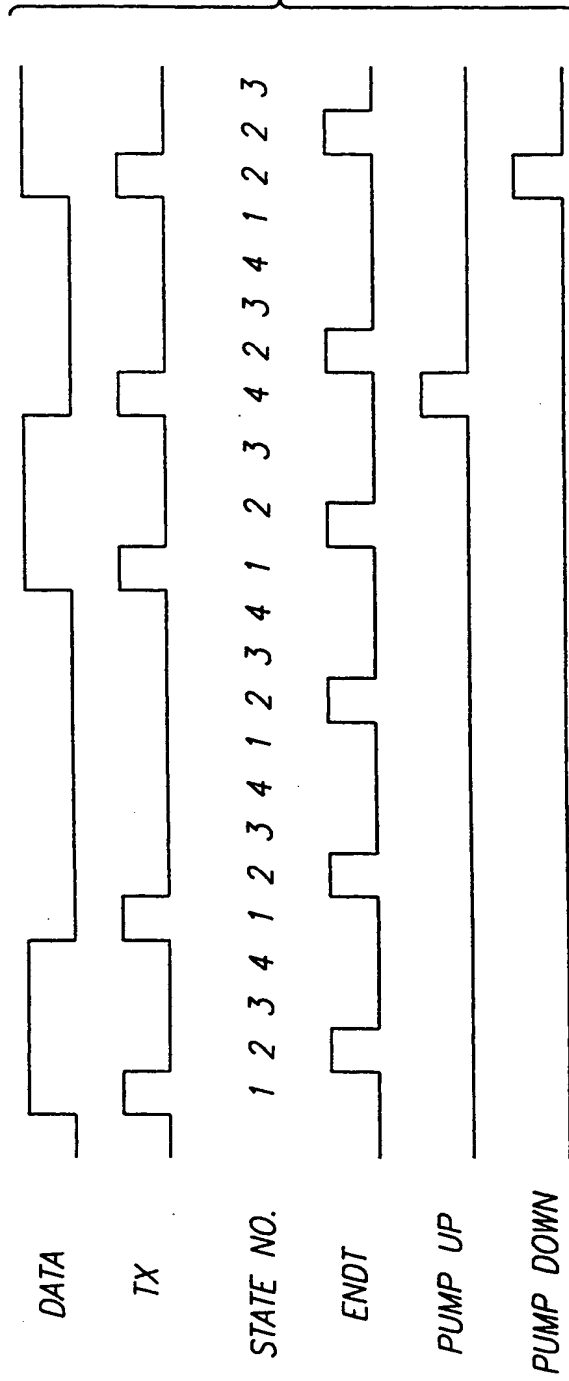
IEEE 68



IEEE 69



IEEE 70



IIII



NAME	CURRENT ( $\mu$ A)	$\Delta V$ (mV)	$\Delta V/V$ CONTROL(NOM) X 100
COARSE	40	160	13.3%
MEDIUM	10	40	3.3
MEDIUM FINE	1	2.6	0.22
FINE	0.1	0.26	0.022

II 09 72